

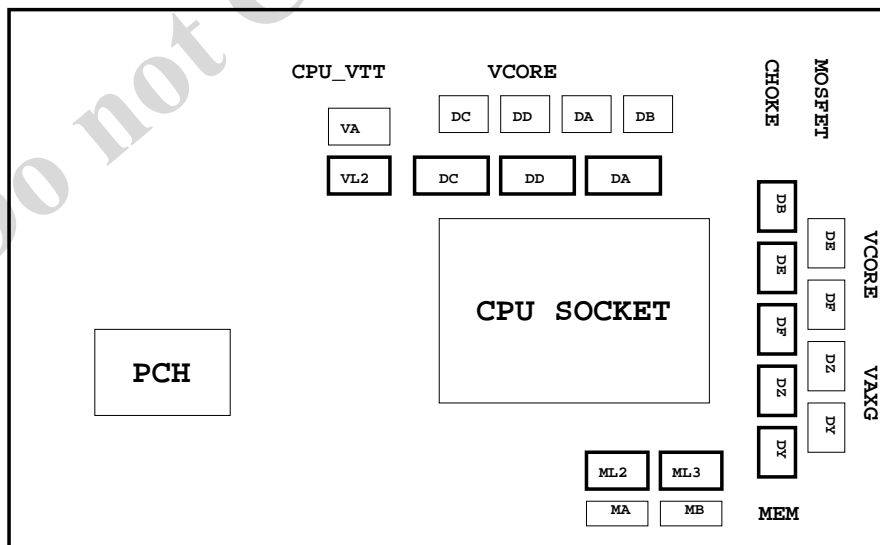
Model Name: GA-Z77X-UD3H

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP_HDMI_DVI_DAC,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*4 SLOT / SWITCH
19	IT8892 PCIE to PCI BRIDGE
20	PCI SLOT
21	DP / HDMI / DVI Connector
22	mSATA Connector
23	Dual BIOS , TPM
24	VT2021
25	REAR AUDIO JACK
26	VCORE PWM_IR3567-1
27	VCORE PWM_IR3567-2

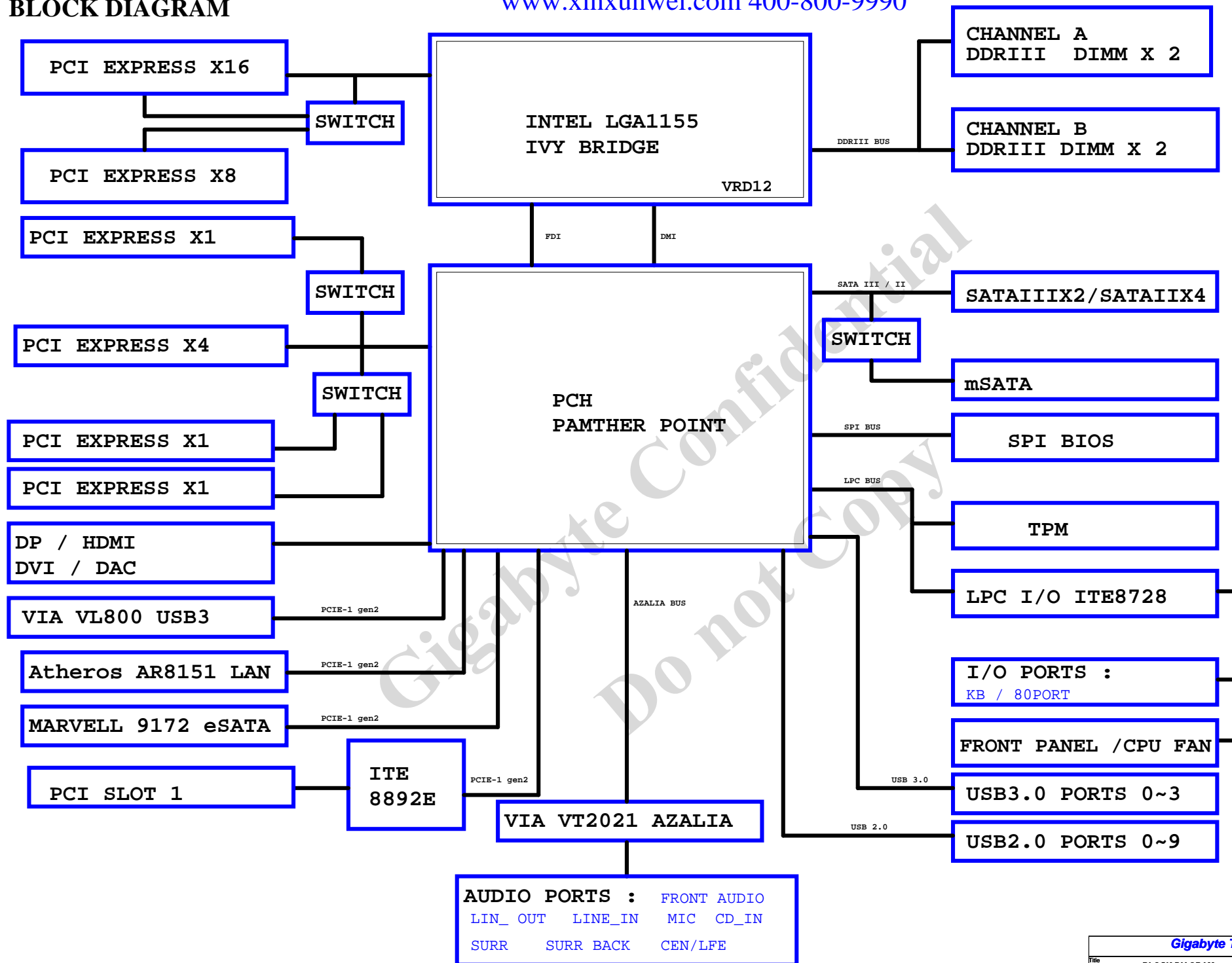
SHEET TITLE

28	DDR_15V & CPUVTT PWM_IR3570-1
29	DDR_15V & CPUVTT PWM_IR3570-2
30	DISCRETE POWER 1
31	DISCRETE POWER 2
32	I/O IT8728F
33	USB3_ESATA , KB/USB3, -PHOT
34	F_PANEL , F_USB , F_USB3
35	ATX POWER, CLOCK GEN
36	HWM, FAN CTRL
37	Atheros 8151
38	ESATA SE9172
39	80PORT / PWR SW / OV NCT3933
40	VIA VL800
41	TABLE LIST



BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990





LGA1155A

M_AA0	AV27	SA_MA[0]
M_AA1	AY24	SA_MA[1]
M_AA2	AW24	SA_MA[2]
M_AA3	AW23	SA_MA[3]
M_AA4	AV23	SA_MA[4]
M_AA5	AT24	SA_MA[5]
M_AA6	AT23	SA_MA[6]
M_AA7	AU22	SA_MA[7]
M_AA8	AV22	SA_MA[8]
M_AA9	AT22	SA_MA[9]
M_AA10	AV28	SA_MA[10]
M_AA11	AU21	SA_MA[11]
M_AA12	AT21	SA_MA[12]
M_AA13	AW32	SA_MA[13]
M_AA14	AU20	SA_MA[14]
M_AA15	AT20	SA_MA[15]

(7) M_SWEA	M_SCASA	AW29	SA_WE#
(7) M_SCASA	M_SRASA	AV30	SA_CAS#
(7) M_SRASA		AU28	SA_RAS#
(7) M_SBA0	M_SBA0	AY29	SA_BS[0]
(7) M_SBA1	M_SBA1	AW28	SA_BS[1]
(7) M_SBA2	M_SBA2	AV20	SA_BS[2]
(7) M-CSA0	M-CSA0	AU29	SA_CS#0
(7) M-CSA1	M-CSA1	AV32	SA_CS#1
(7) M-CSA2	M-CSA2	AW30	SA_CS#2
(7) M-CSA3	M-CSA3	AU33	SA_CS#3
(7) M_CKEA0	M_CKEA0	AV19	SA_CKE[0]
(7) M_CKEA1	M_CKEA1	AT19	SA_CKE[1]
(7) M_CKEA2	M_CKEA2	AU18	SA_CKE[2]
(7) M_CKEA3	M_CKEA3	AV18	SA_CKE[3]
(7) M_ODT_A0		AV31	SA_ODT[0]
(7) M_ODT_A1		AU32	SA_ODT[1]
(7) M_ODT_A2		AU30	SA_ODT[2]
(7) M_ODT_A3		AW33	SA_ODT[3]

(7) M_DCLKA0	M_DCLKA0	AY25	SA_CK[0]
(7) M_DCLKA0	M_DCLKA0	AW25	SA_CK[0]
(7) M_DCLKA1	M_DCLKA1	AU24	SA_CK[1]
(7) M_DCLKA1	M_DCLKA1	AU25	SA_CK[1]
(7) M_DCLKA2	M_DCLKA2	AW27	SA_CK[2]
(7) M_DCLKA2	M_DCLKA2	AY27	SA_CK[2]
(7) M_DCLKA3	M_DCLKA3	AU26	SA_CK[3]
(7) M_DCLKA3	M_DCLKA3	AW26	SA_CK[3]

(7,8) M_DDR3_RST < MR1 04/SHT/MX
MBC8 0.1u4/X7R/16V/KX

AV13	SA_DQS[8]
AV12	SA_DQS#8
AU12	SA_ECC_CB[0]
AU14	SA_ECC_CB[1]
AW13	SA_ECC_CB[2]
AY13	SA_ECC_CB[3]
AU13	SA_ECC_CB[4]
AY12	SA_ECC_CB[5]
AW12	SA_ECC_CB[6]
AW12	SA_ECC_CB[7]

DDR_0

1 OF 10

LGA1155[10SC1-F01155-01R]

AK3	M_DQSA0
AK2	M_DQSA0
AJ3	M_DA0
AJ4	M_DA1
AL4	M_DA2
AL4	M_DA3
AJ2	M_DA4
SA_DQ[4]	M_DA5
SA_DQ[5]	M_DA6
SA_DQ[6]	M_DA7
SA_DQ[7]	
AP3	M_DQSA1
AP2	M_DQSA1

AN1	M_DA8
AN4	M_DA9
AR3	M_DA10
AR4	M_DA11
AN2	M_DA12
AN3	M_DA13
AR2	M_DA14
AR1	M_DA15

AW4	M_DQSA2
AW4	M_DQSA2

AV2	M_DA16
AW3	M_DA17
AV5	M_DA18
AW5	M_DA19
AU2	M_DA20
AJ3	M_DA21
AJ5	M_DA22
AY5	M_DA23

AV8	M_DQSA3
AW8	M_DQSA3

AY7	M_DA24
AU7	M_DA25
AV9	M_DA26
AU9	M_DA27
AV7	M_DA28
AW7	M_DA29
AW9	M_DA30
AY9	M_DA31

AV37	M_DQSA4
AV36	M_DQSA4

AU35	M_DA32
AW37	M_DA33
AU39	M_DA34
AU36	M_DA35
AW35	M_DA36
AY36	M_DA37
AU38	M_DA38
AU37	M_DA39

AP38	M_DQSA5
AP39	M_DQSA5

AR40	M_DA40
AR37	M_DA41
AN38	M_DA42
AN37	M_DA43
AR39	M_DA44
AR38	M_DA45
AN39	M_DA46
AN40	M_DA47

AK38	M_DQSA6
AK39	M_DQSA6

AL40	M_DA48
AL37	M_DA49
AJ38	M_DA50
AJ37	M_DA51
AL39	M_DA52
AL38	M_DA53
AJ39	M_DA54
AJ40	M_DA55

AF38	M_DQSA7
AF39	M_DQSA7

AG40	M_DA56
AG37	M_DA57
AE38	M_DA58
AE37	M_DA59
AG39	M_DA60
AG38	M_DA61
AE39	M_DA62
AE40	M_DA63

(7) M_ODT_A[0..3]	M_ODT_A[0..3]
(8) M_ODT_B[0..3]	M_ODT_B[0..3]
(7) M_DA[0..63]	M_DA[0..63]
(8) M_DB[0..63]	M_DB[0..63]
(7) M_DQSA[0..7]	M_DQSA[0..7]
(7) M_DQSA[0..7]	M_DQSA[0..7]
(7) M_DQSA[0..7]	M_DQSA[0..7]
(7) M_AA[0..15]	M_AA[0..15]
(8) M_AA[0..15]	M_AA[0..15]
(8) M_DQSB[0..7]	M_DQSB[0..7]
(8) M_DQSB[0..7]	M_DQSB[0..7]

LGA1155B

M_AAB0	AK24	SB_MA[0]
M_AAB1	AM20	SB_MA[1]
M_AAB2	AM19	SB_MA[2]
M_AAB3	AK18	SB_MA[3]
M_AAB4	AP19	SB_MA[4]
M_AAB5	AP18	SB_MA[5]
M_AAB6	AM18	SB_MA[6]
M_AAB7	AL18	SB_MA[7]
M_AAB8	AN18	SB_MA[8]
M_AAB9	AY17	SB_MA[9]
M_AAB10	AN23	SB_MA[10]
M_AAB11	AU17	SB_MA[11]
M_AAB12	AT18	SB_MA[12]
M_AAB13	AR26	SB_MA[13]
M_AAB14	AY16	SB_MA[14]
M_AAB15	AV16	SB_MA[15]

(8) M_SWEB	M_SWEB	AR25	SB_WE#
(8) M_SCASB	M_SCASB	AK25	SB_CAS#
(8) M_SRASB	M_SRASB	AP24	SB_RAS#

(8) M_SBA0	M_SBA0	AP23	SB_BS[0]
(8) M_SBA1	M_SBA1	AM22	SB_BS[1]
(8) M_SBA2	M_SBA2	AW17	SB_BS[2]

(8) M-CSB0	M-CSB0	AN25	SB_CS#0
(8) M-CSB1	M-CSB1	AN26	SB_CS#1
(8) M-CSB2	M-CSB2	AL25	SB_CS#2
(8) M-CSB3	M-CSB3	AT26	SB_CS#3

(8) M_CKEB0	M_CKEB0	AU16	SB_CKE[0]
(8) M_CKEB1	M_CKEB1	AY15	SB_CKE[1]
(8) M_CKEB2	M_CKEB2	AW15	SB_CKE[2]
(8) M_CKEB3	M_CKEB3	AV15	SB_CKE[3]

(8) M_ODT_B0	M_ODT_B0	AL26	SB_ODT[0]
(8) M_ODT_B1	M_ODT_B1	AP26	SB_ODT[1]
(8) M_ODT_B2	M_ODT_B2	AK26	SB_ODT[2]
(8) M_ODT_B3	M_ODT_B3	AK26	SB_ODT[3]

(8) M_DCLKB0	M_DCLKB0	AL21	SB_CK[0]
(8) M_DCLKB0	M_DCLKB0	AL22	SB_CK[0]
(8) M_DCLKB1	M_DCLKB1	AL20	SB_CK[1]
(8) M_DCLKB1	M_DCLKB1	AK20	SB_CK[1]
(8) M_DCLKB2	M_DCLKB2	AL23	SB_CK[2]
(8) M_DCLKB2	M_DCLKB2	AM22	SB_CK[2]
(8) M_DCLKB3	M_DCLKB3	AP21	SB_CK[3]
(8) M_DCLKB3	M_DCLKB3	AN21	SB_CK[3]

(8) M_VREF_DQB	AH1	FC_AH1
(7) M_VREF_DQA	AH4	FC_AH4

AN16	SB_DQS[8]
AN15	SB_DQS#8

AL16	SB_ECC_CB[0]
AM16	SB_ECC_CB[1]
AP16	SB_ECC_CB[2]
AL15	SB_ECC_CB[3]
AM15	SB_ECC_CB[4]
AP15	SB_ECC_CB[5]
AP15	SB_ECC_CB[7]

AL33	M_DQSB6
AM33	M_DQSB6

DDR_1

2 OF 10

LGA1155[10SC1-F01155-01R]

SB_DQS[0]	AH7	M_DQSB0
SB_DQS#0	AH6	M_DQSB0
SB_DQ[0]	AG7	M_DB0
SB_DQ[1]	AG8	M_DB1
SB_DQ[2]	AJ9	M_DB2
SB_DQ[3]	AJ8	M_DB3
SB_DQ[4]	AG5	M_DB4
SB_DQ[5]	AG6	M_DB5
SB_DQ[6]	AJ6	M_DB6
SB_DQ[7]	AJ7	M_DB7
SB_DQS[11]	AM8	M_DQSB1
SB_DQS#11	AL8	M_DQSB1

SB_WE#	AM7	M_DB8
SB_CAS#	AM7	M_DB9
SB_RAS#	AM10	M_DB10
SB_BS[0]	AL10	M_DB11
SB_BS[1]	AL6	M_DB12
SB_BS[2]	AM6	M_DB13
SB_BS[2]	AL9	M_DB14
SB_BS[2]	AM9	M_DB15

SB_CS#0	AR8	M_DQSB2
SB_CS#1	AP8	M_DQSB2
SB_CS#2		
SB_CS#3		

SB_CKE[0]	AP7	M_DB16
SB_CKE[1]	AR7	M_DB17
SB_CKE[2]	AP10	M_DB18
SB_CKE[3]	AR10	M_DB19
SB_ODT[0]	AP6	M_DB20
SB_ODT[1]	AR6	M_DB21
SB_ODT[2]	AP9	M_DB22
SB_ODT[3]	AR9	M_DB23

SB_DQS[3]	AN13	M_DQSB3
SB_DQS#3	AN12	M_DQSB3

SB_CK[0]	AM12	M_DB24
SB_CK[0]	AM13	M_DB25
SB_CK[1]	AR13	M_DB26
SB_CK[1]	AP13	M_DB27
SB_CK[2]	AL12	M_DB28
SB_CK[2]	AL13	M_DB29
SB_CK[3]	AR12	M_DB30
SB_CK[3]	AP12	M_DB31

SB_DQS[4]	AN29	M_DQSB4
SB_DQS#4	AN28	M_DQSB4

SB_DQ[32]	AR28	M_DB32
SB_DQ[33]	AR29	M_DB33
SB_DQ[34]	AL28	M_DB34
SB_DQ[35]	AL29	M_DB35
SB_DQ[36]	AP28	M_DB36
SB_DQ[37]	AP29	M_DB37
SB_DQ[38]	AM28	M_DB38
SB_DQ[39]	AM29	M_DB39

SB_DQS[5]	AP33	M_DQSB5
SB_DQS#5	AR33	M_DQSB5

SB_DQ[40]	AP32	M_DB40
SB_DQ[41]	AP31	M_DB41
SB_DQ[42]	AP35	M_DB42
SB_DQ[43]	AP34	M_DB43
SB_DQ[44]	AR32	M_DB44
SB_DQ[45]	AR31	M_DB45
SB_DQ[46]	AR35	M_DB46
SB_DQ[47]	AR34	M_DB47

SB_DQS[6]	AL33	M_DQSB6
SB_DQS#6	AM33	M_DQSB6

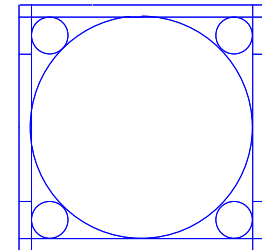
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SB_DQ[49]	AM31	M_DB49
SB_DQ[50]	AL35	M_DB50
SB_DQ[51]	AL32	M_DB51
SB_DQ[52]	AM34	M_DB52
SB_DQ[53]	AL31	M_DB53
SB_DQ[54]	AM35	M_DB54
SB_DQ[55]	AL34	M_DB55

SB_DQS[7]	AG35	M_DQSB7
SB_DQS#7	AG34	M_DQSB7

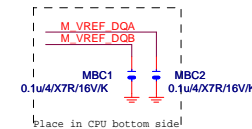
SB_DQ[56]	AH35	M_DB56
SB_DQ[57]	AH34	M_DB57
SB_DQ[58]	AE34	M_DB58
SB_DQ[59]	AE35	M_DB59
SB_DQ[60]	AJ35	M_DB60
SB_DQ[61]	AJ34	M_DB61
SB_DQ[62]	AF33	M_DB62
SB_DQ[63]	AF35	M_DB63

LGA1155

ILM_BP/1156/BKNI

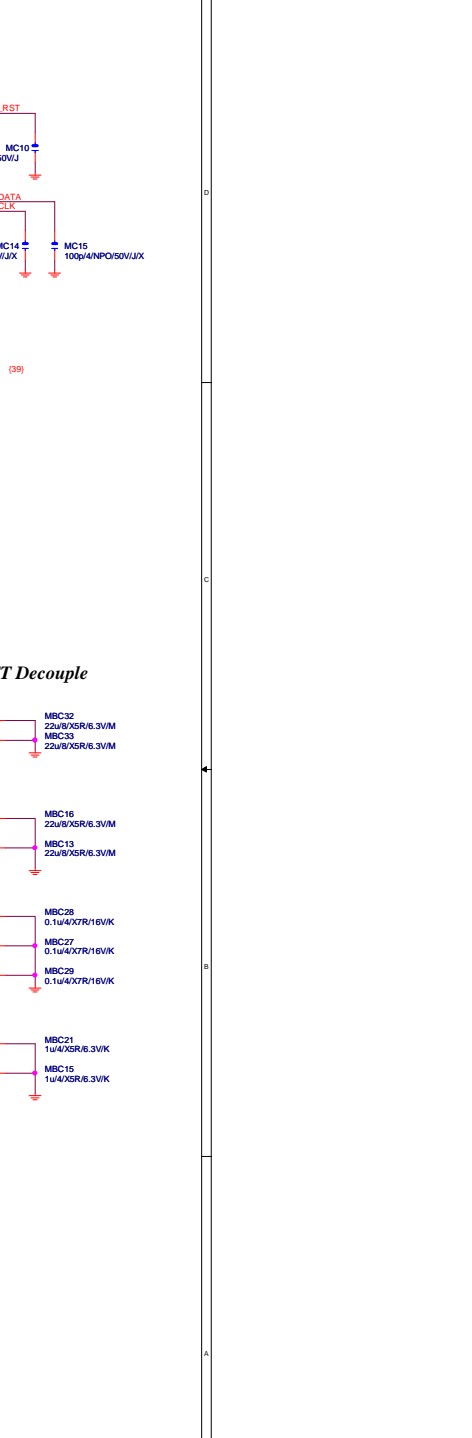
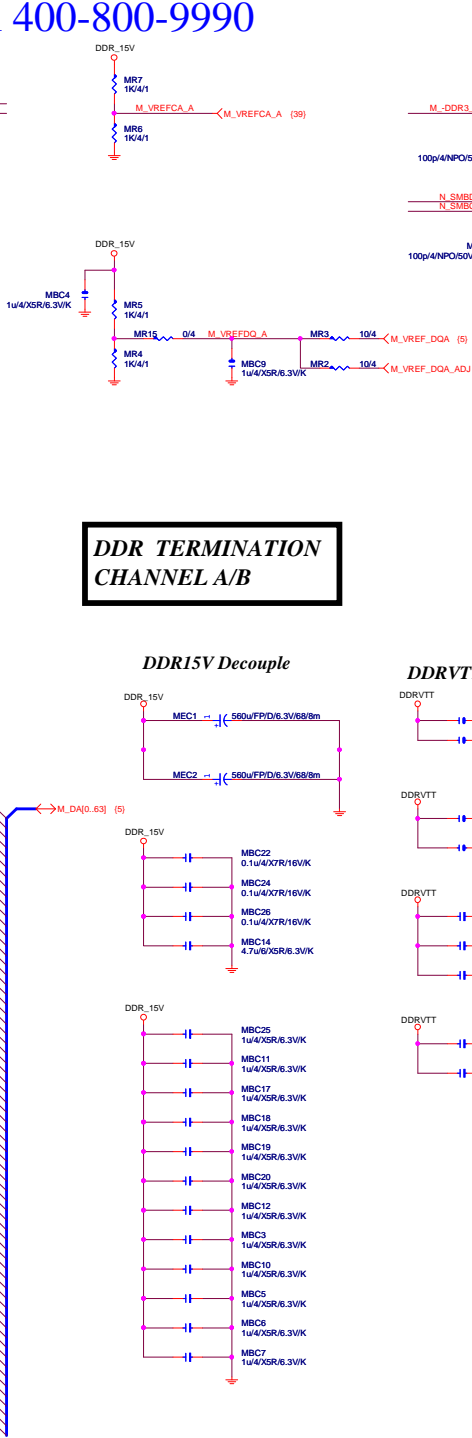
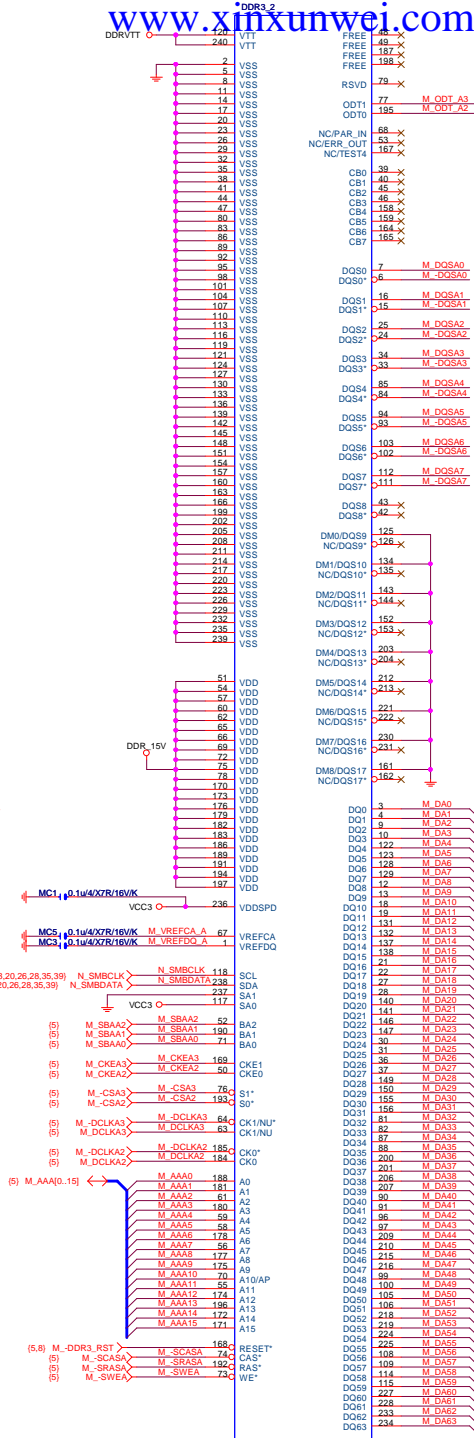
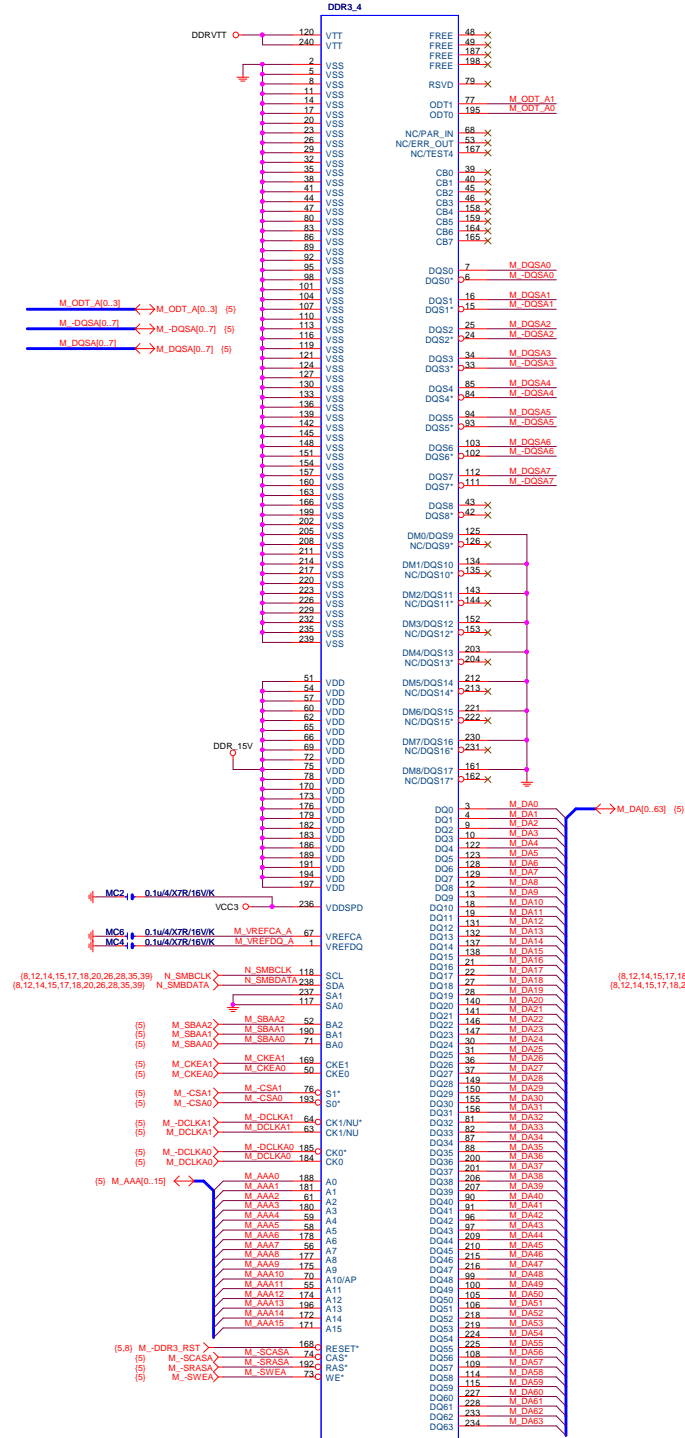


Need check the new CPU ME



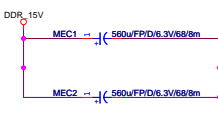
Intel CRB

Title			CPU LGA1156-B		
Size			Document Number		
Custom			GA-Z77X-UD3H		
Date:			Wednesday, March 21, 2012		
Sheet			5 of 41		
Rev			1.03		

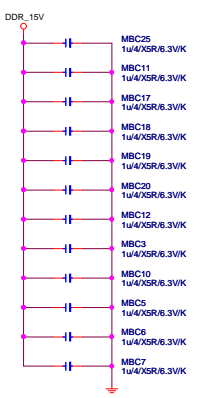
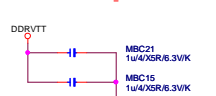
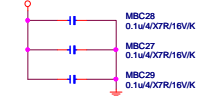
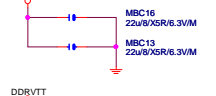
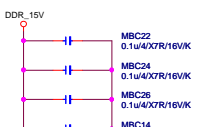
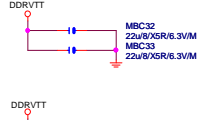


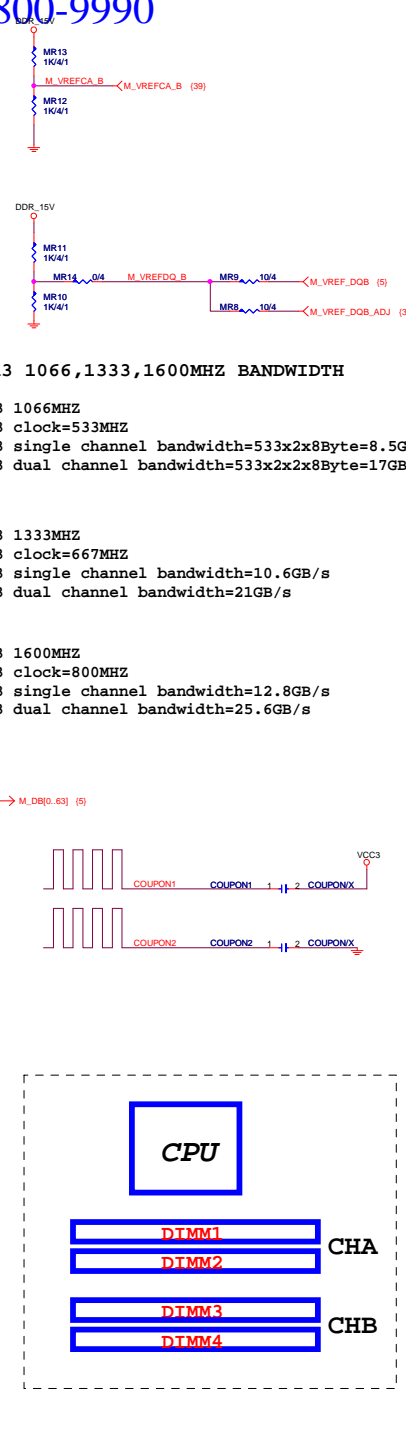
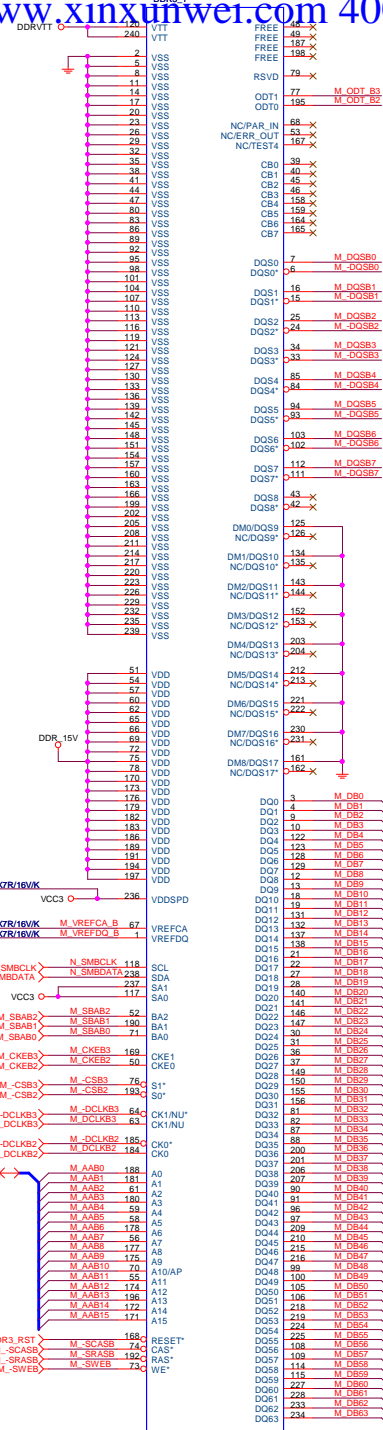
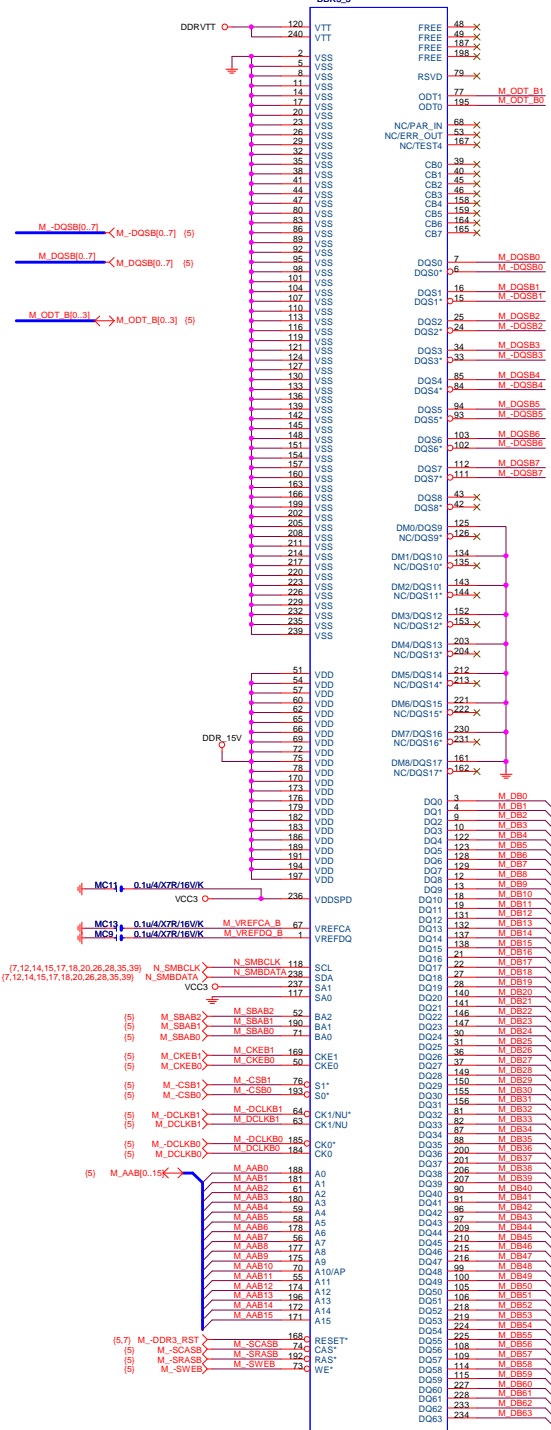
DDR TERMINATION CHANNEL A/B

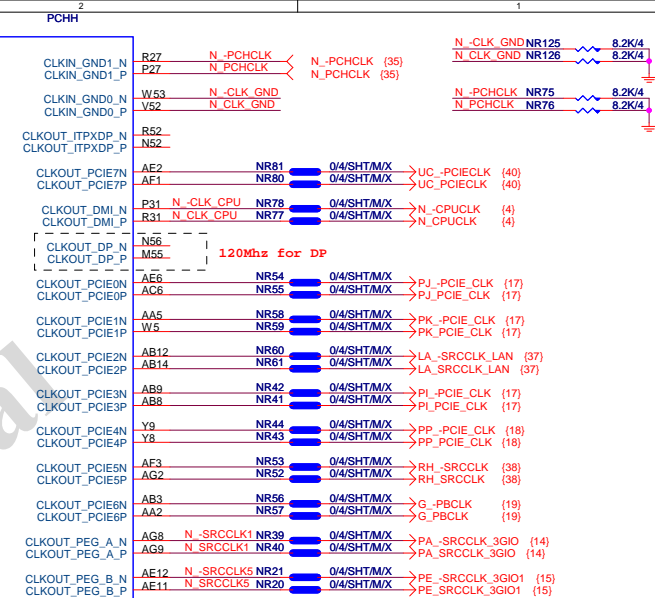
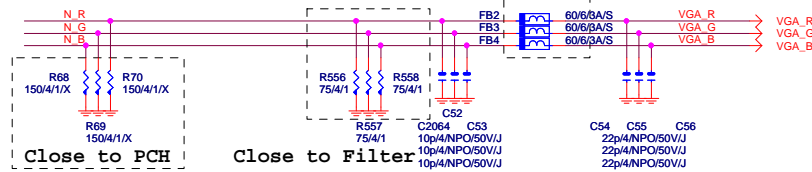
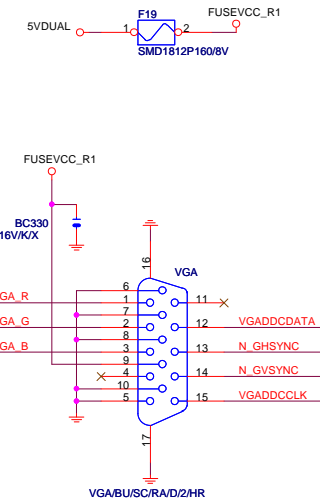
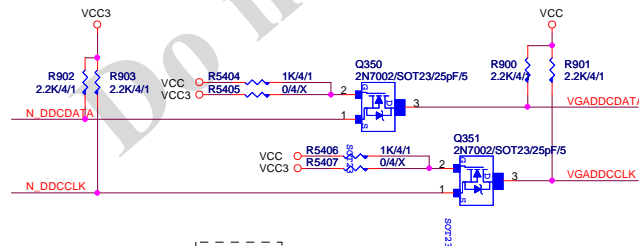
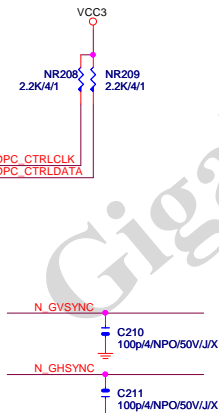
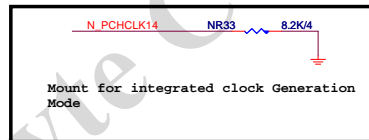
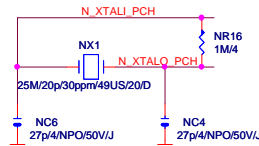
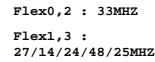
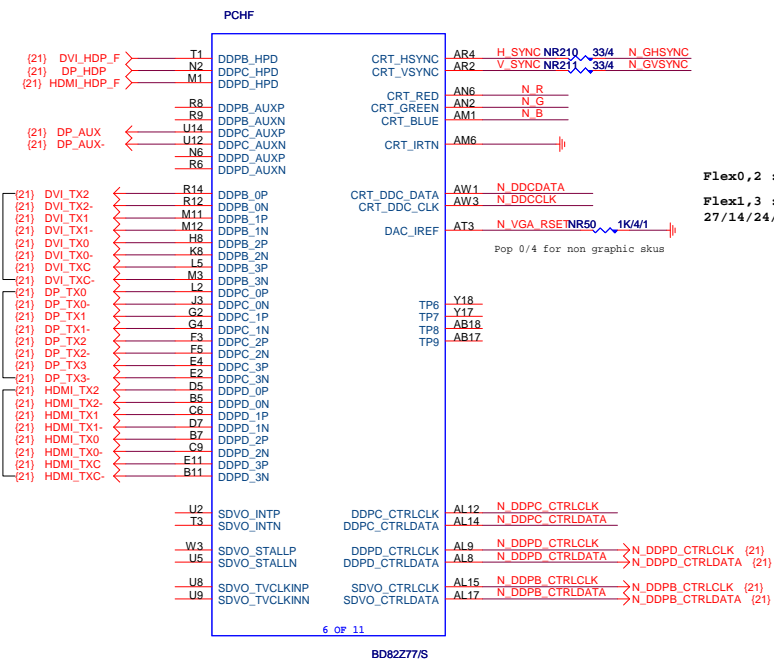
DDR15V Decouple



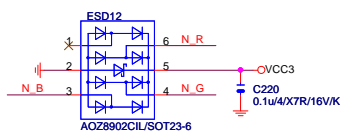
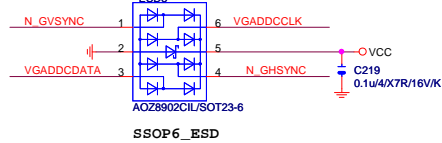
DDRVTT Decouple

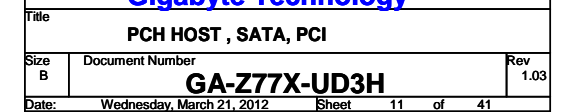




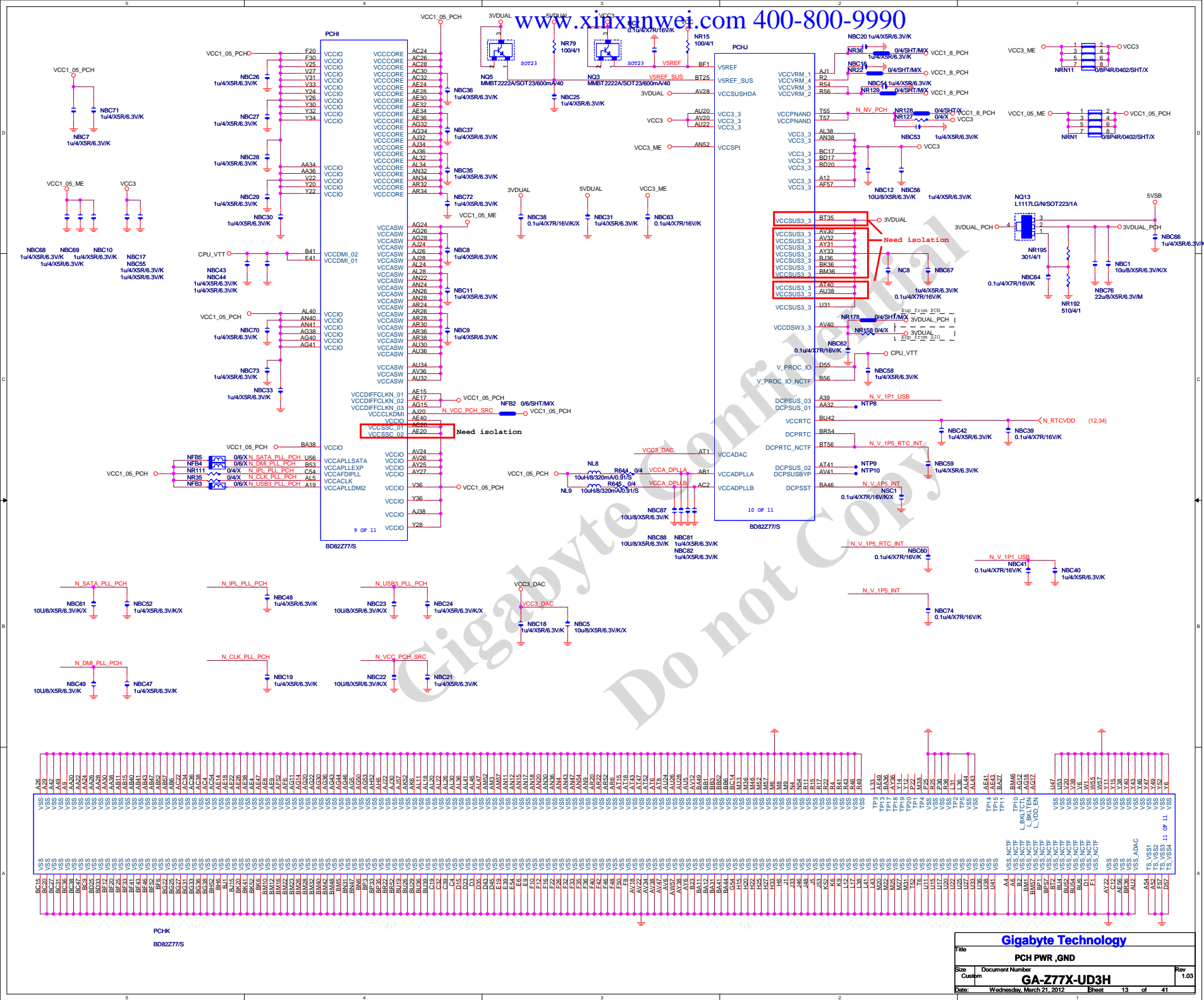


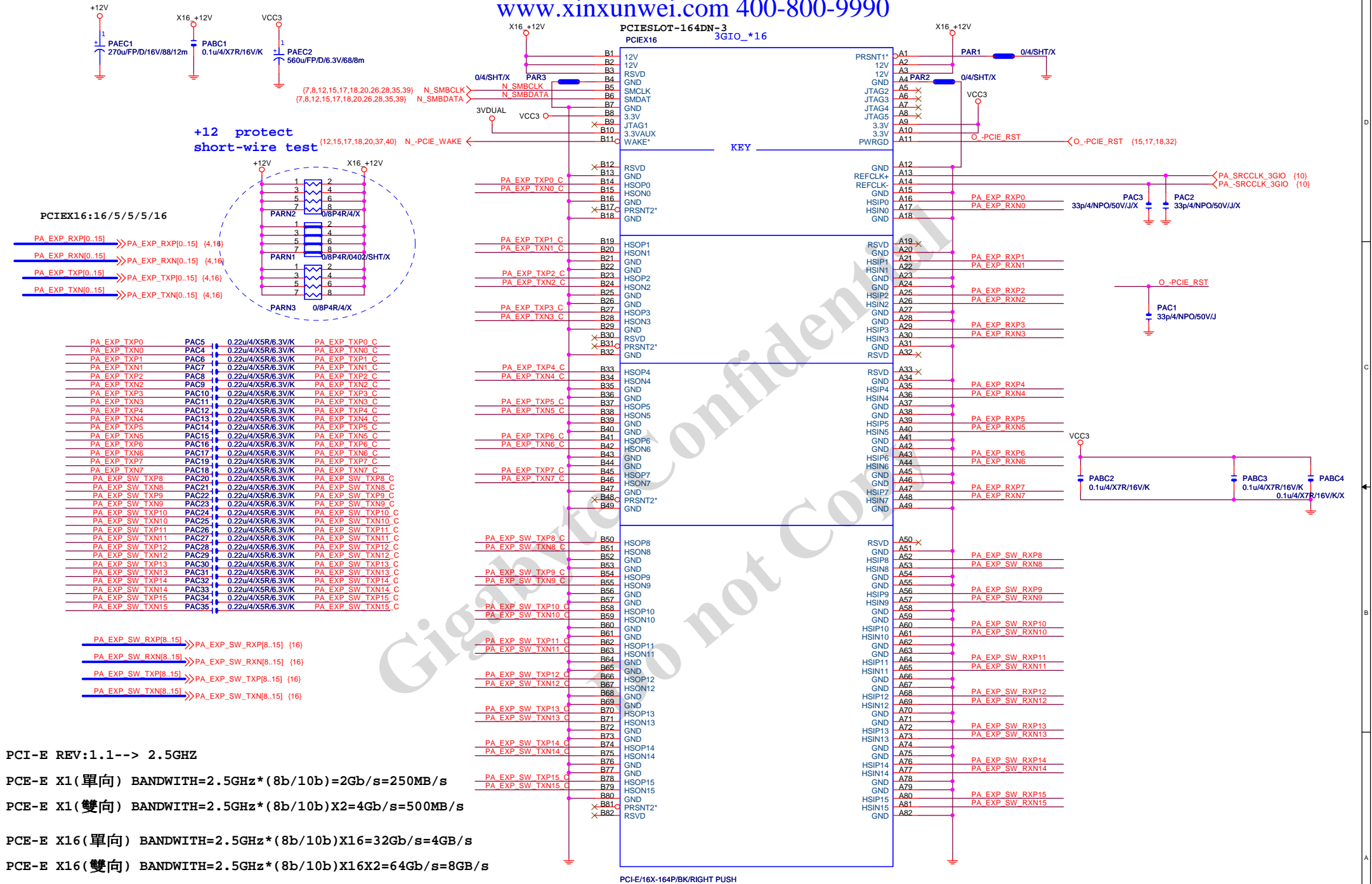
Differential Clock:18/6/4/6/18
Impedance=90 +- 15%





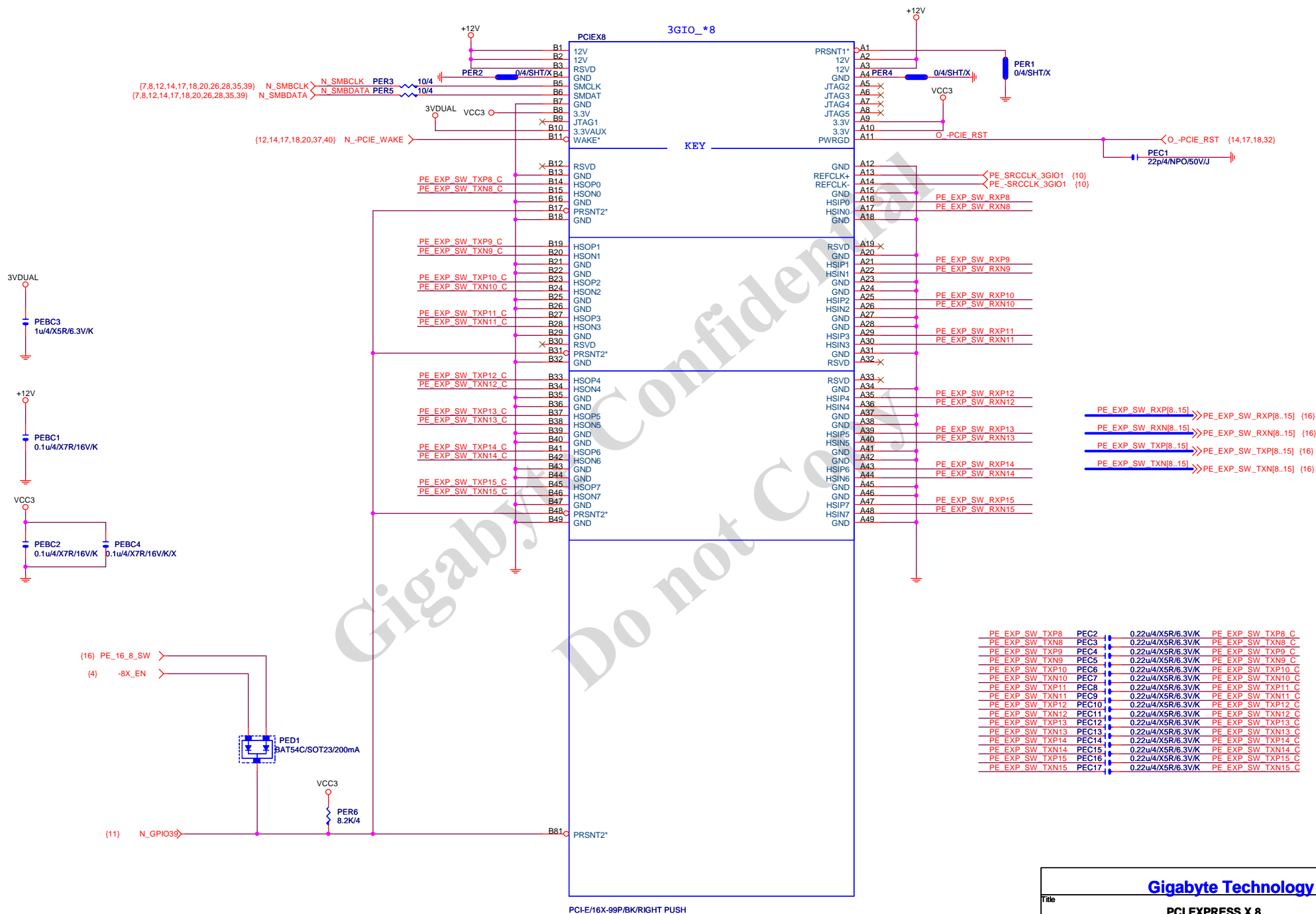


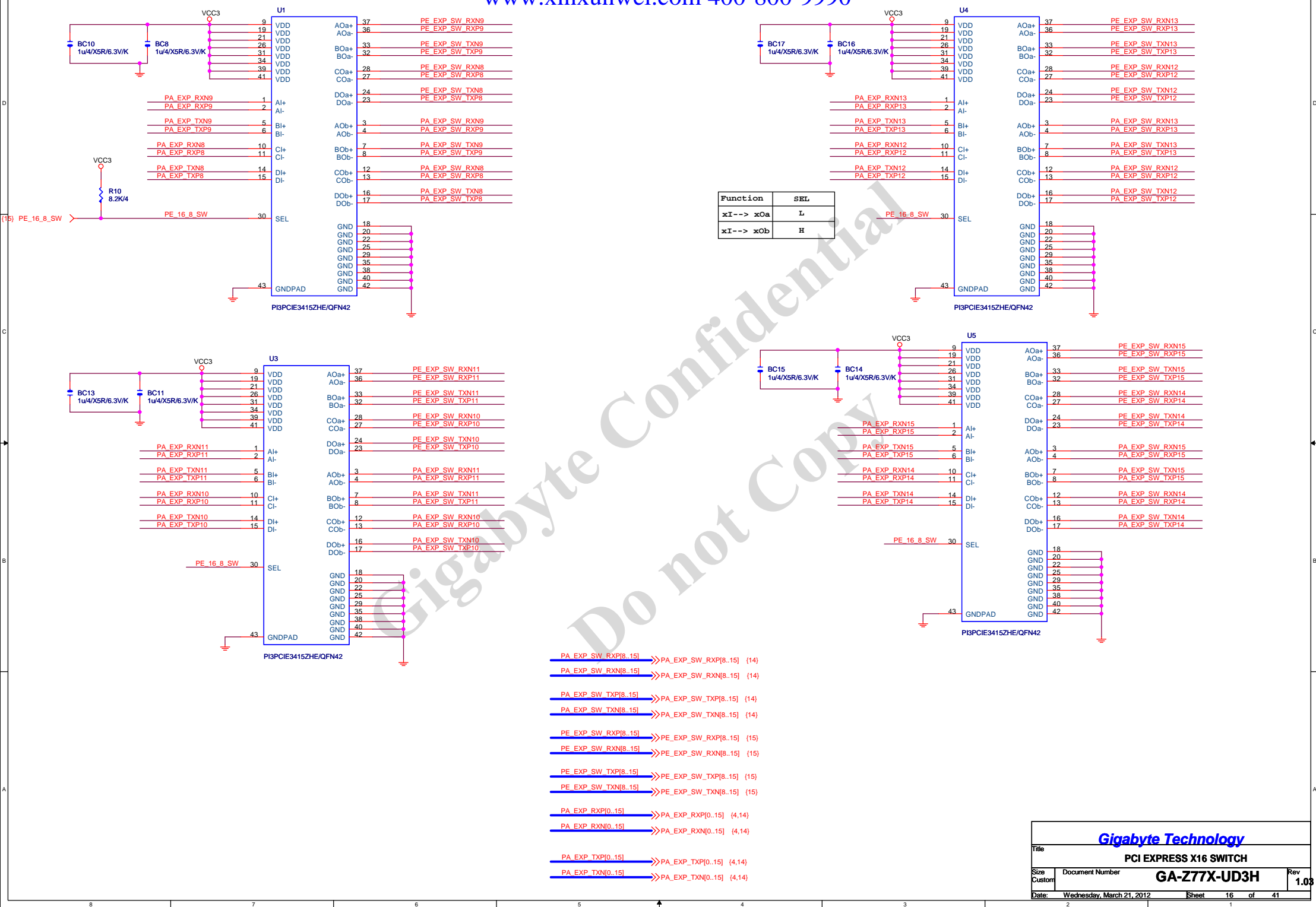




Gigabyte Technology

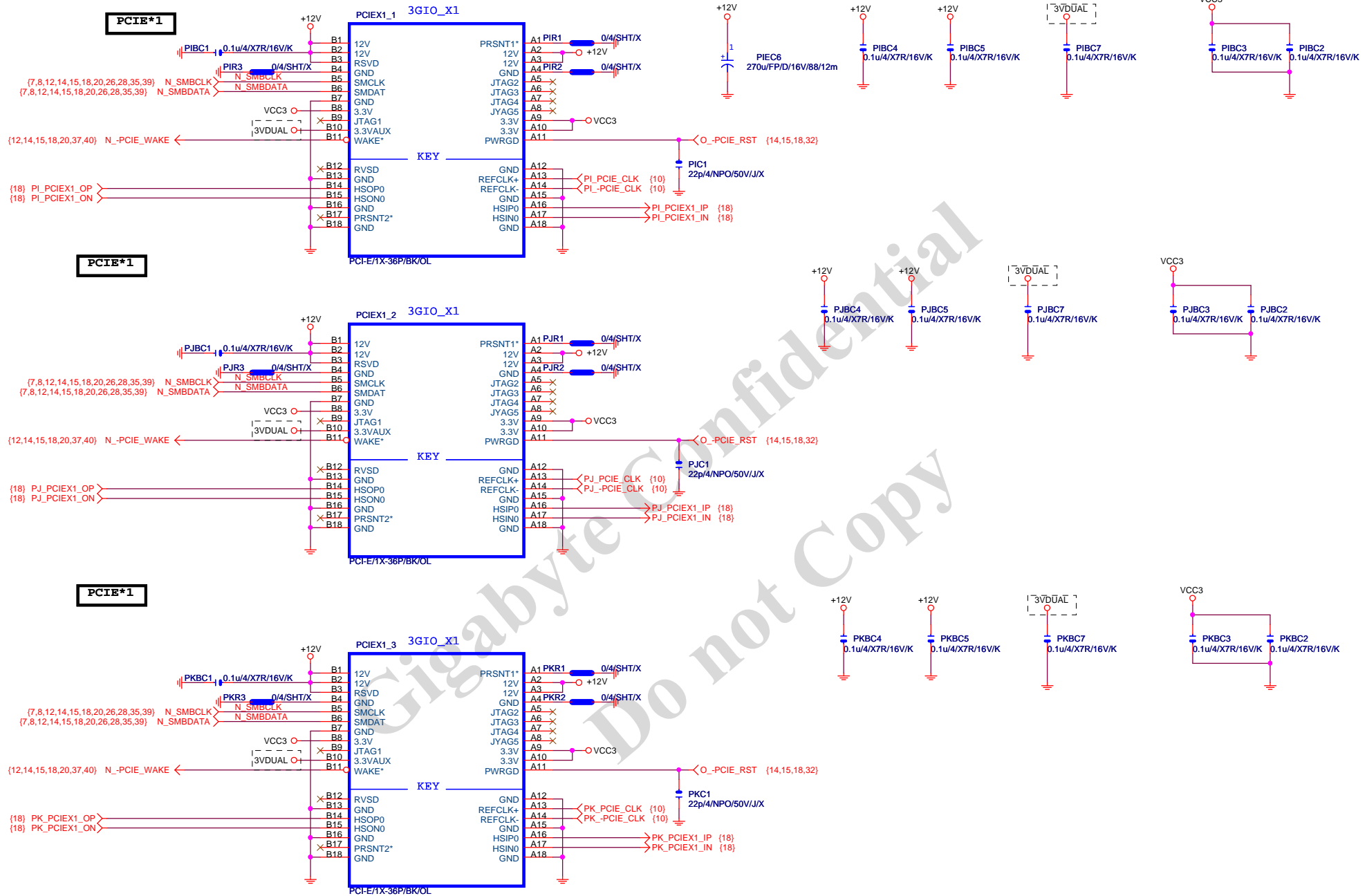
Title			PCI EXPRESS X 16
Size	Document Number	GA-Z77X-UD3H	
Custom		Rev	1.03
Date:	Wednesday, March 21, 2012	Sheet	14 of 41





Gigabyte Technology

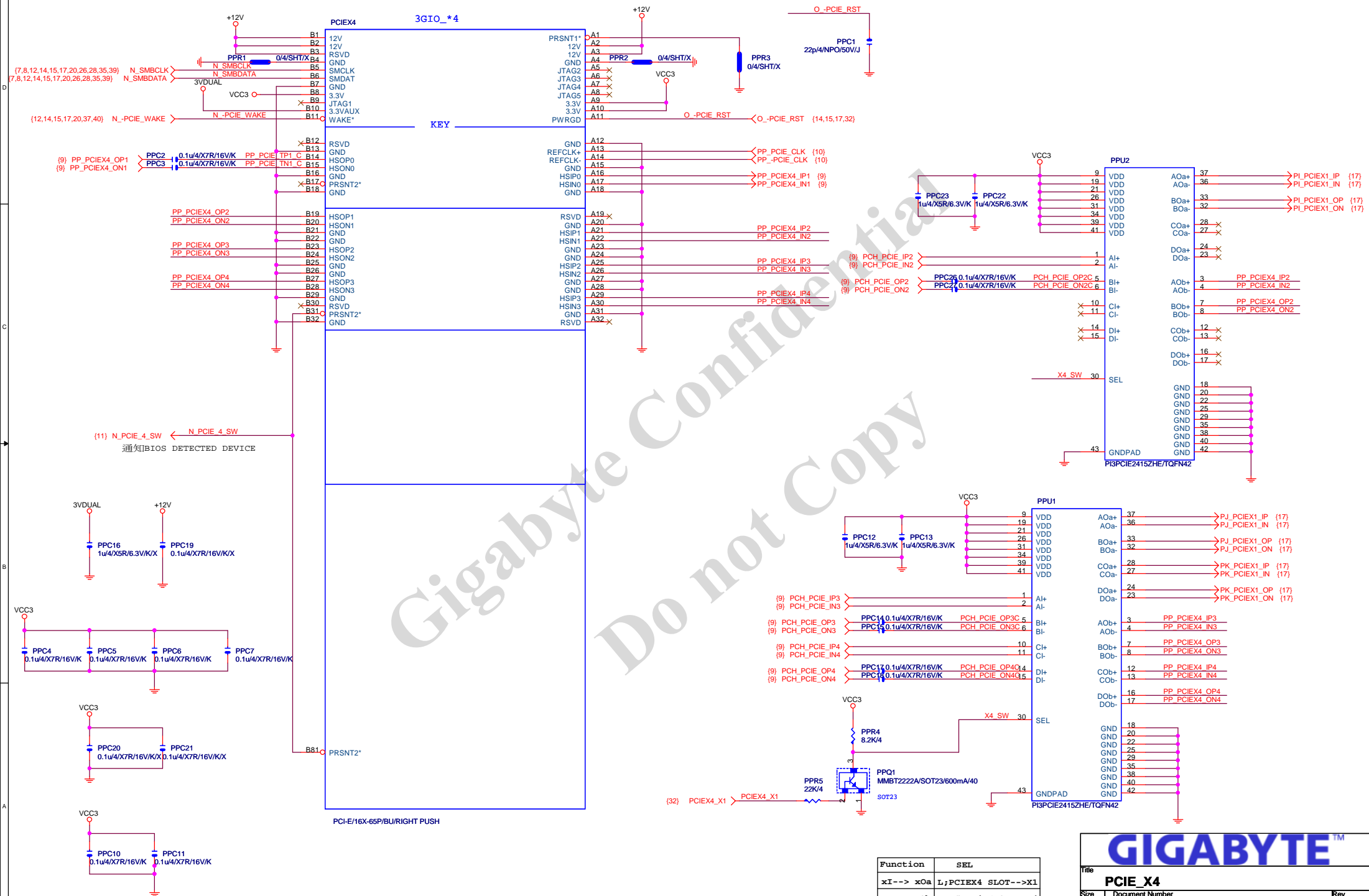
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Size	Document Number	GA-Z77X-UD3H	
Custom			Rev 1.03
Date:	Wednesday, March 21, 2012	Sheet	16 of 41



Gigabyte Technology

Title			PCIE_X1 1,2,3
Size	Document Number	Rev	
Custom		1.03	
Date:	Wednesday, March 21, 2012	Sheet	17 of 41

PCIE*4



Function	SEL
xI--> xOa	L;PCIE*4 SLOT-->X1
xI--> xOb	H;PCIE*4 SLOT-->X4

GIGABYTE™

Title: **PCIE_X4**

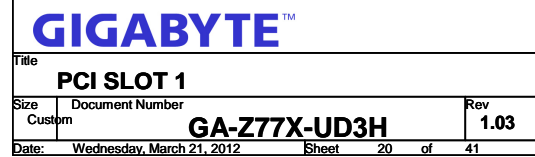
Size: Custom

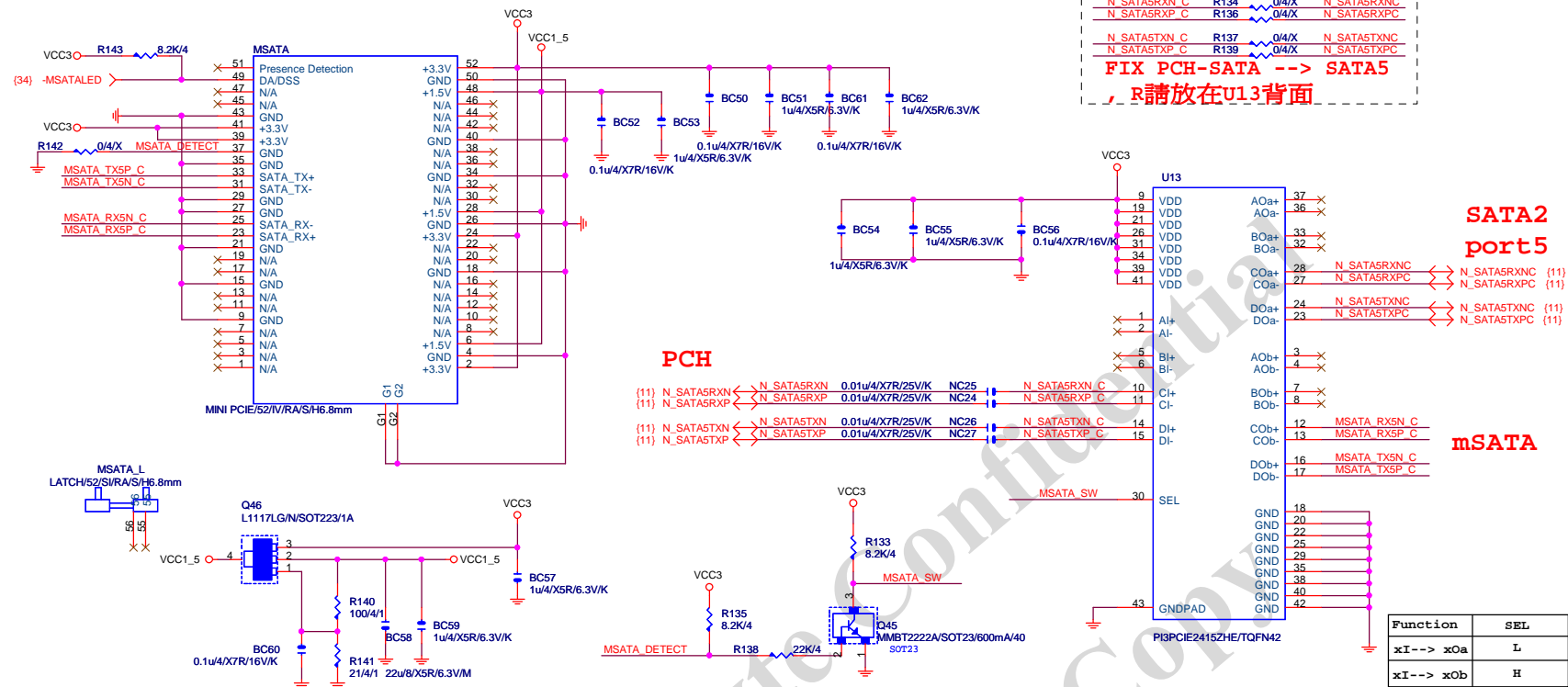
Document Number: **GA-Z77X-UD3H**

Rev: **1.03**

Date: Wednesday, March 21, 2012

Sheet 18 of 41



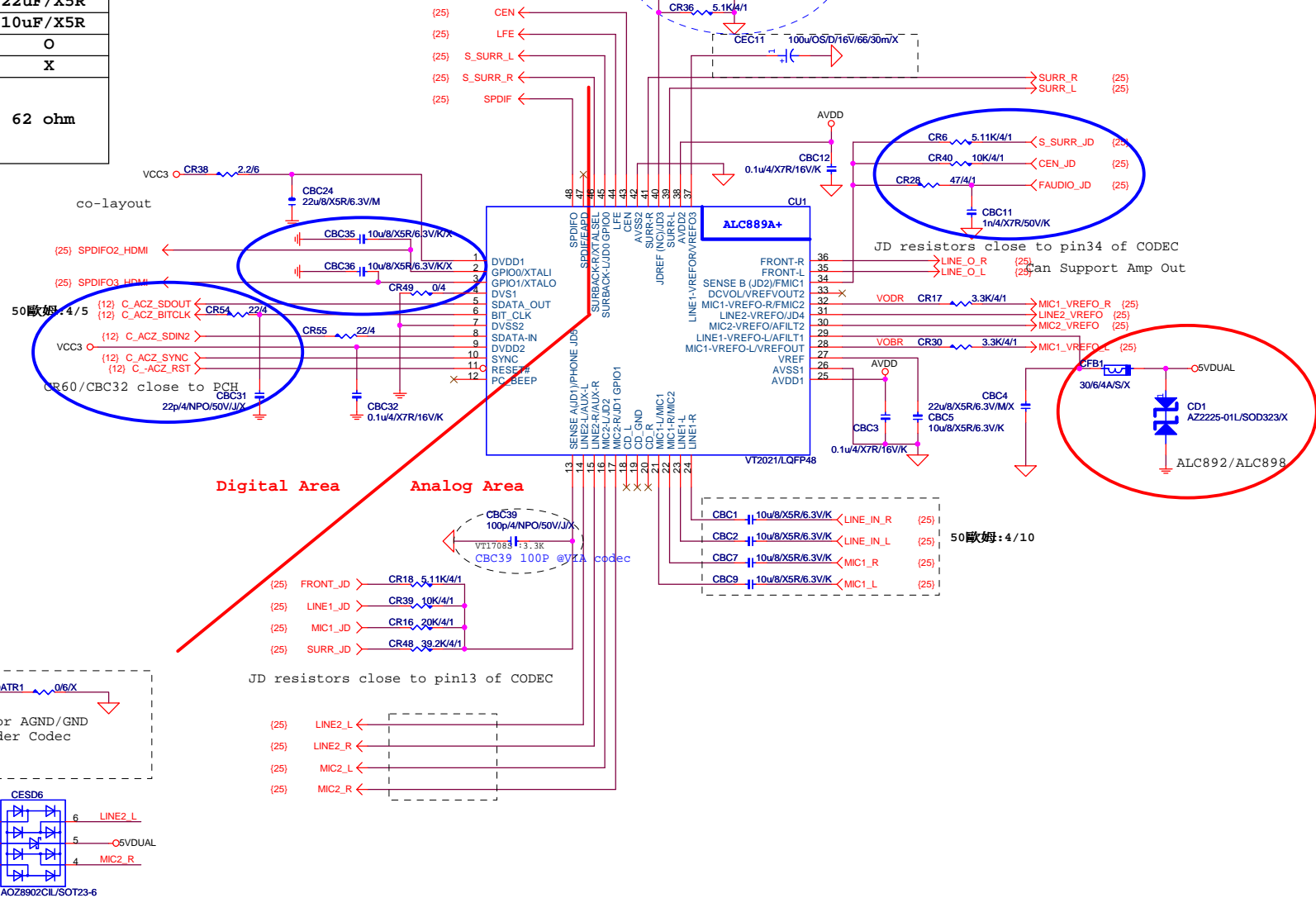


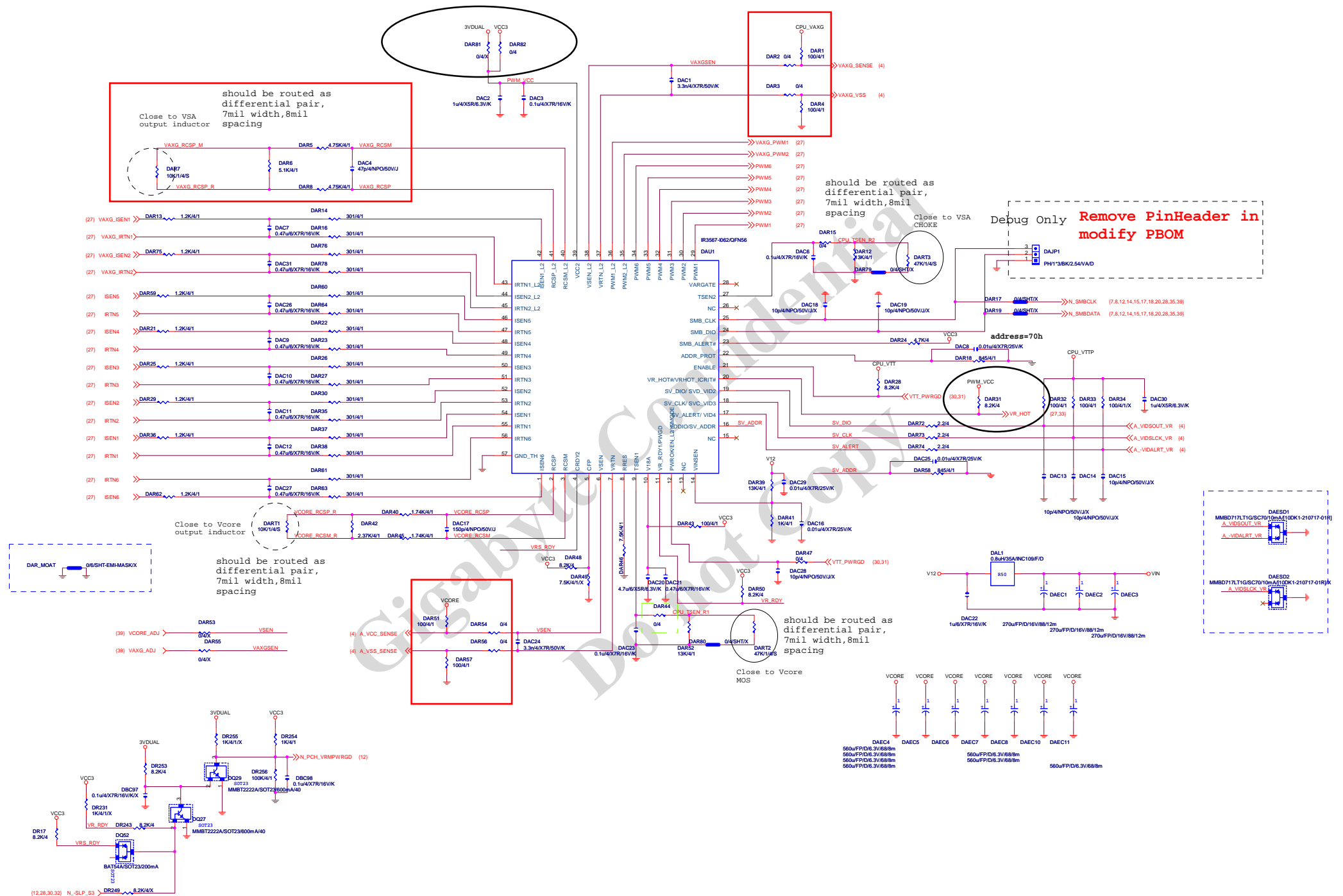


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

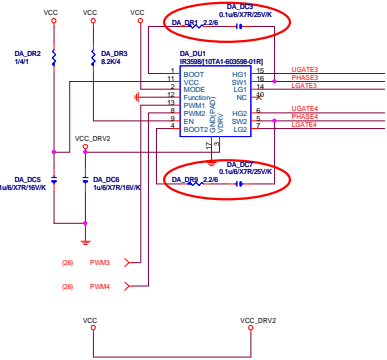
The schematic diagram illustrates the BIOS chip and its associated components. The BIOS chip is connected to VCC and GND. It includes several LEDs (MBIOS_LED, BBIOS_LED) and MOSFETs (Q78, Q79, Q80, Q81, Q82, Q83) for status indication. The chip is also connected to the SPI_HOLD_B and SPI_HOLD_M signals. The TPM module (TPM) is connected to the BIOS chip and provides various signals (LAD0, LAD1, LAD2, LAD3, LAD4, LAD5, LAD6, LAD7, LAD8, LAD9, LAD10, LAD11, LAD12, LAD13, LAD14, LAD15, LAD16, LAD17, LAD18, LAD19, LAD20) to the BIOS chip. The TPM module is also connected to the VCC3 and GND. The BIOS chip is connected to the SPI_HOLD_B and SPI_HOLD_M signals. The TPM module is connected to the VCC3 and GND. The BIOS chip is connected to the SPI_HOLD_B and SPI_HOLD_M signals. The TPM module is connected to the VCC3 and GND.

	ALC889	ALC889B	ALC898/ALC892
CR49	O	O	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	O	X	O
CR53	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	O
CD2/CD3/CQ3/CQ4	O	O	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm





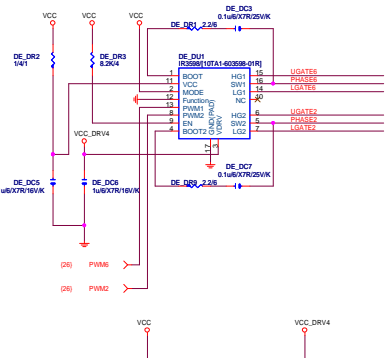
VCORE Phase 3,6



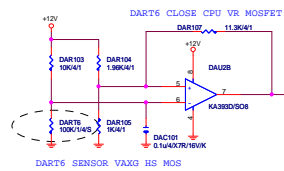
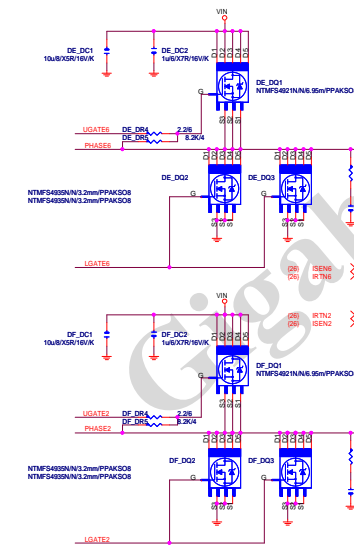
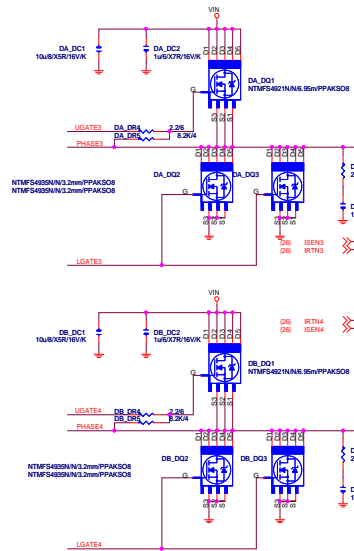
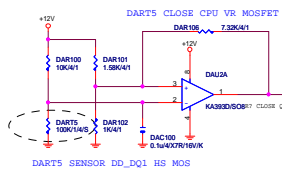
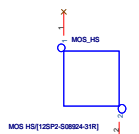
FUNCTION	MODE	PMO MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

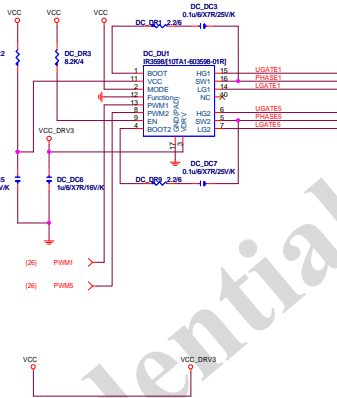
VCORE Phase 5,2



MOS HEATSINK



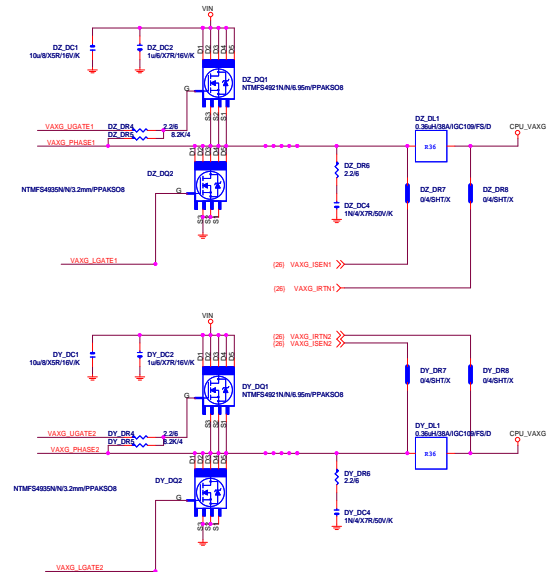
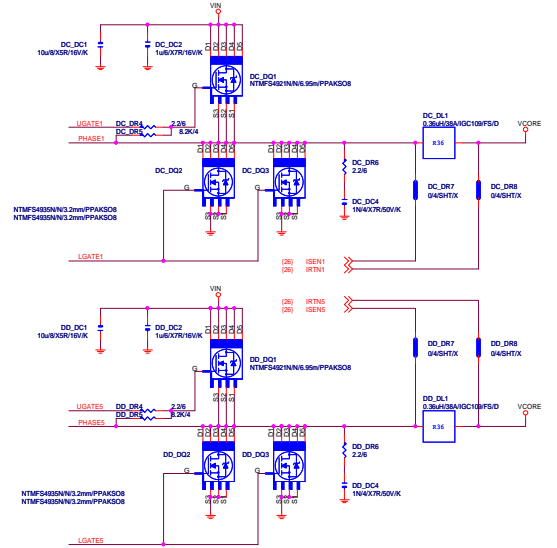
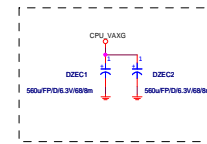
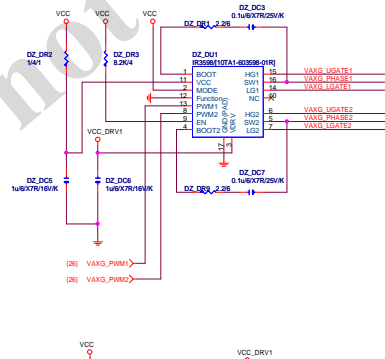
VCORE Phase 1,4

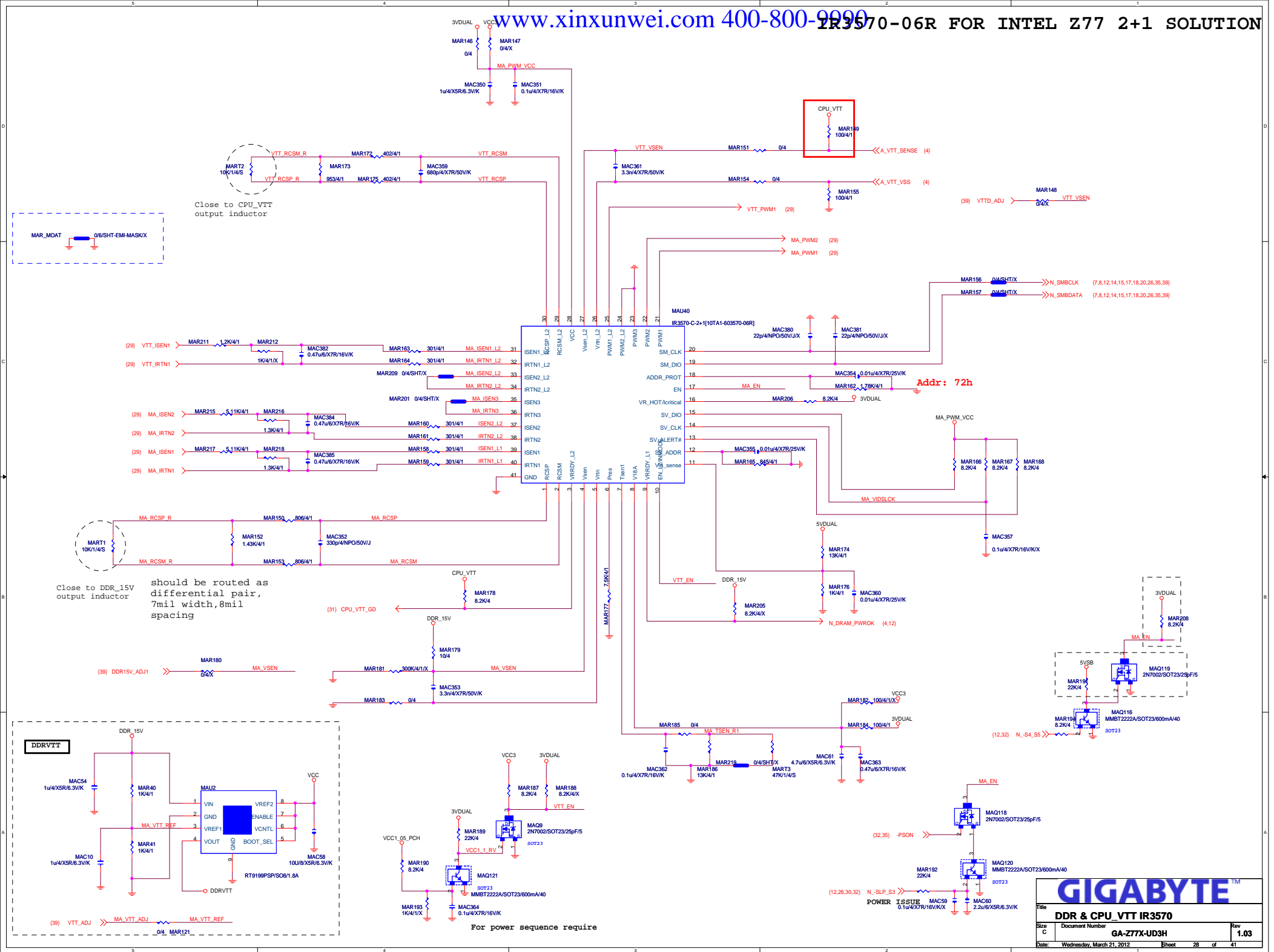


FUNCTION	MODE	PRN MODE	PHASE MODE
0	1	1R ATL	OCAL
1	1	1R ATL	Doubler
0	0	Tri-Seate	OCAL
1	0	Tri-Seate	Doubler
OPEN	0	Tri-Seate	Quad
OPEN	1	1R ATL	Quad

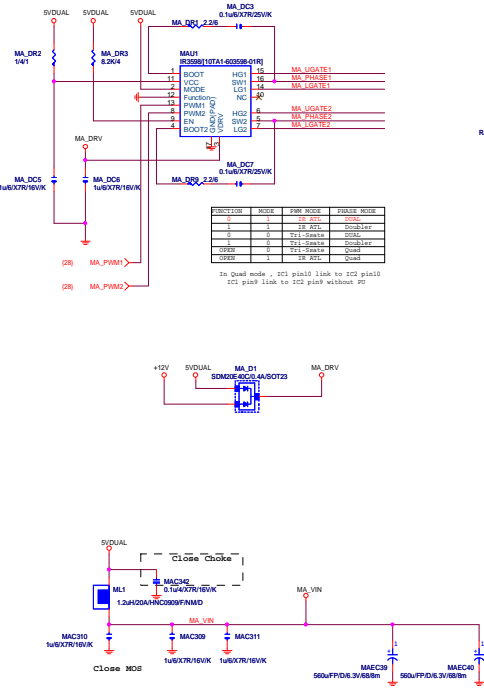
In Quad mode , IC1 pin10 link to IC2 pin
IC1 pin9 link to IC2 pin9 without 5V

VAXG Phase

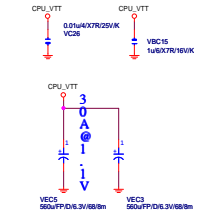
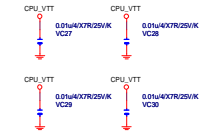
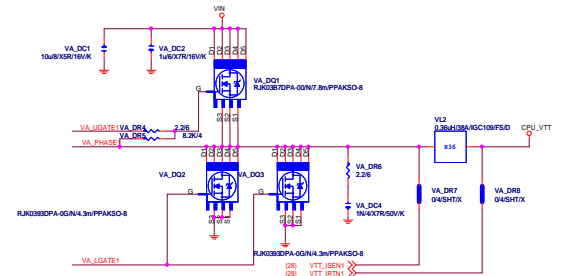
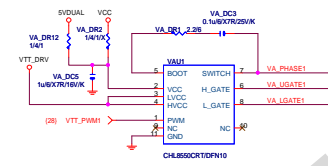


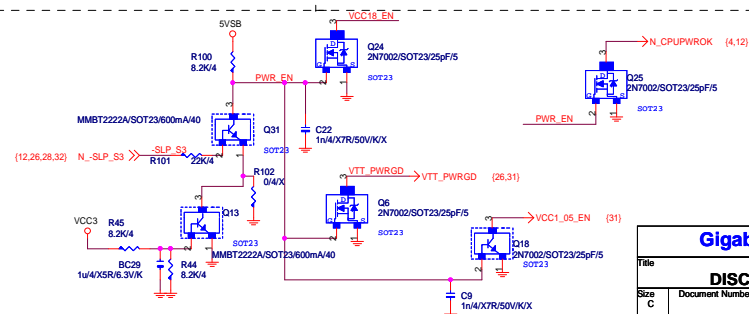
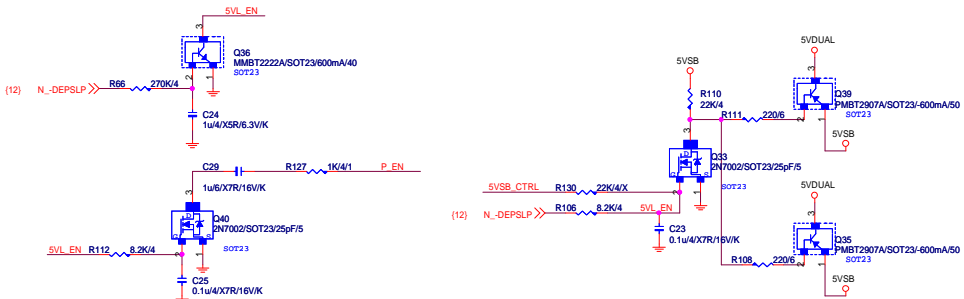
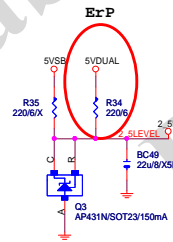
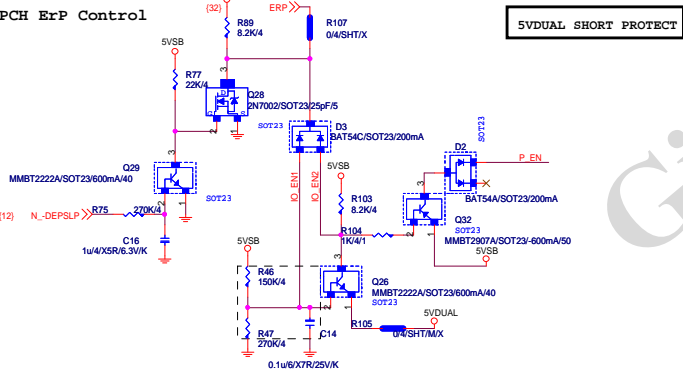
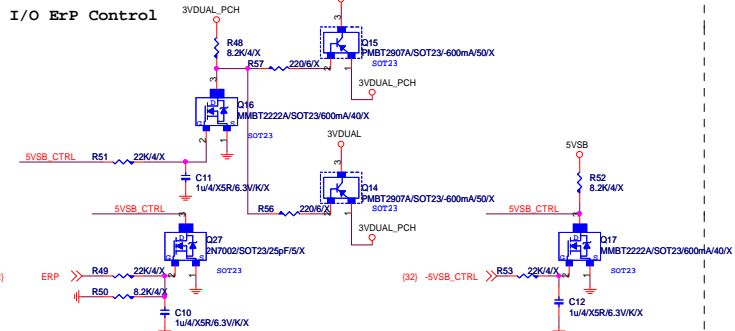
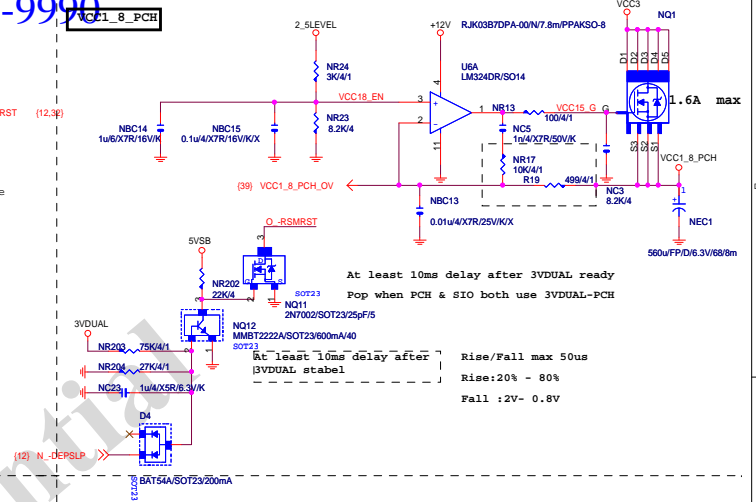
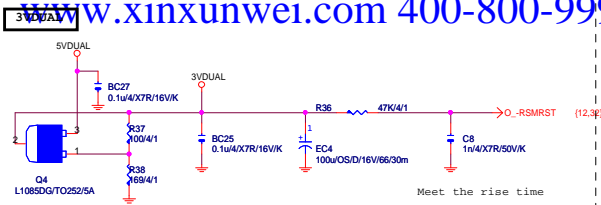
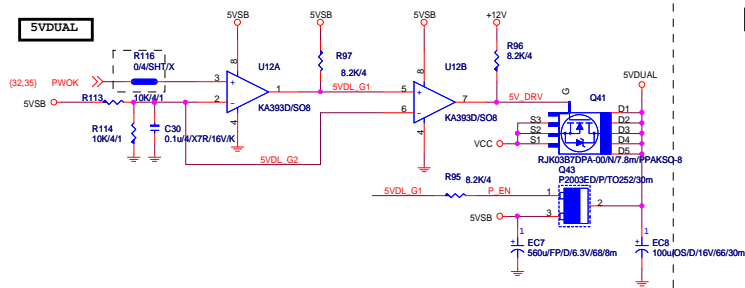


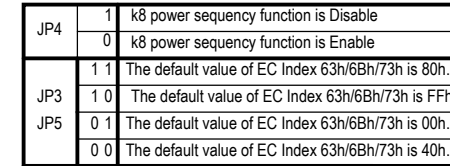
DDR_15V



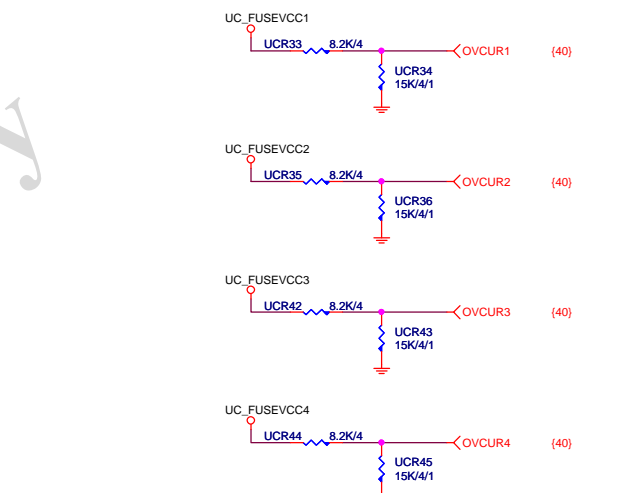
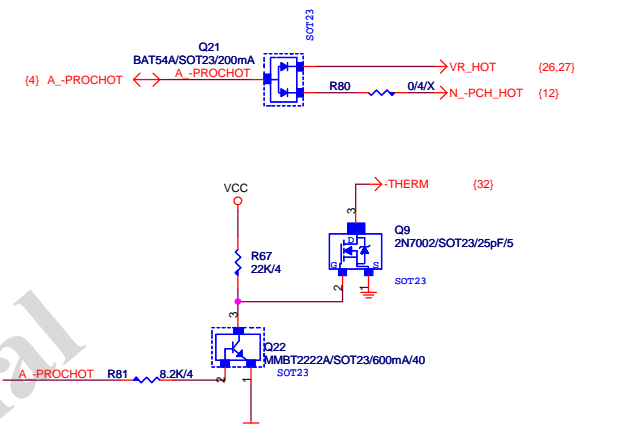
CPU_VTT



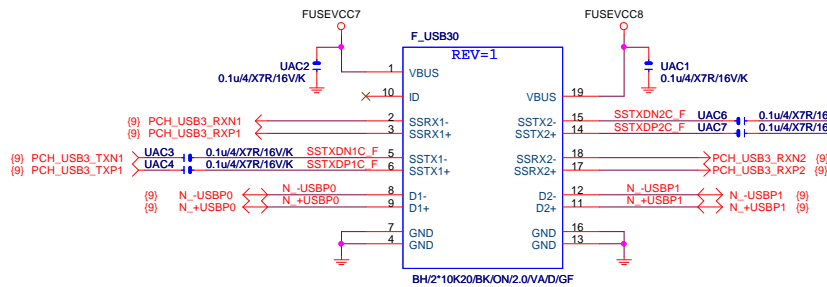




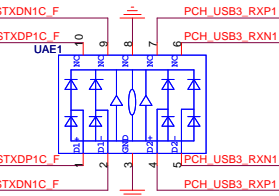
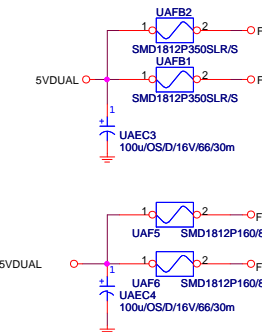
	IT8721	IT8728
PIN121	FAN_CTL4/VID_TURBO	VCORE_EN/PCH_C0
PIN120	VDDA_EN	VLDT_EN/PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST/AMDTSI_D/PECI_AVA/MTRB#/PCH_D	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSI_C/DRVSB/PCH_C	PECI/AMDTSI_C/DRVSB#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3/ATXPG	VIN2(VCC5)
PIN96	VIN2	VIN1(VCC12)
PIN97	VIN1(VCC5)	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0(VCC12)	VIN0/VCORE(1.1V)



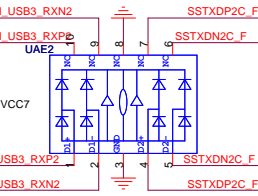
CASE OPEN



(9,12) N_GPIO11 ← N_USBOC_F

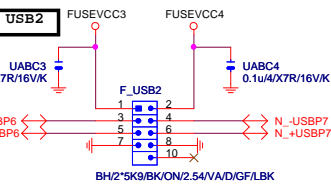


Close to connector

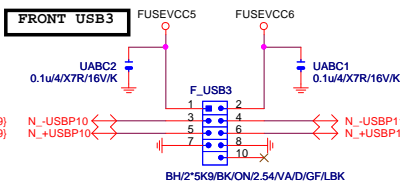


Close to connector

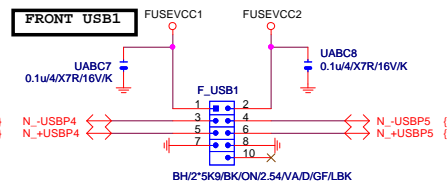
Close to connector



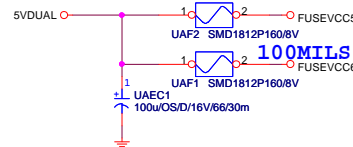
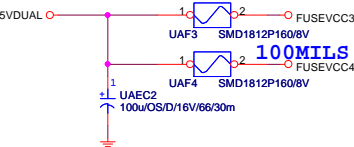
Close to connector



Close to connector



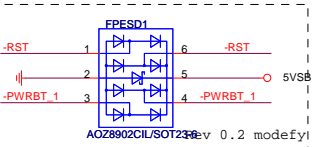
Close to connector



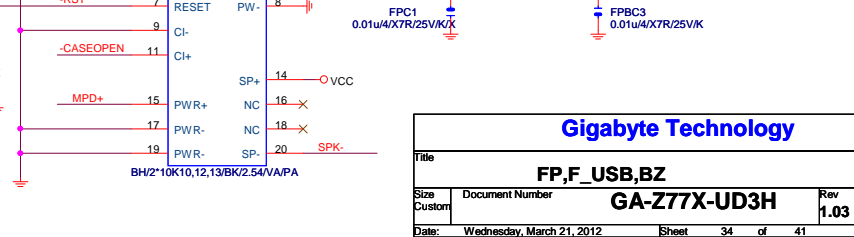
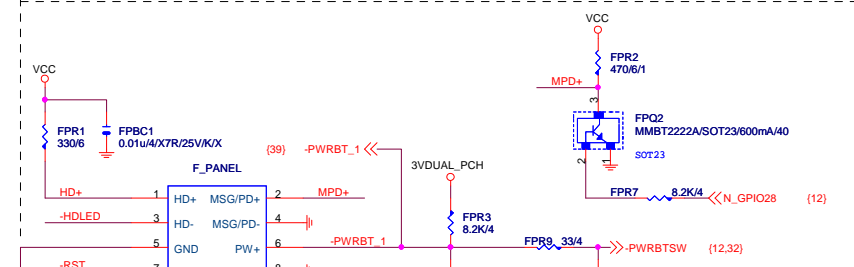
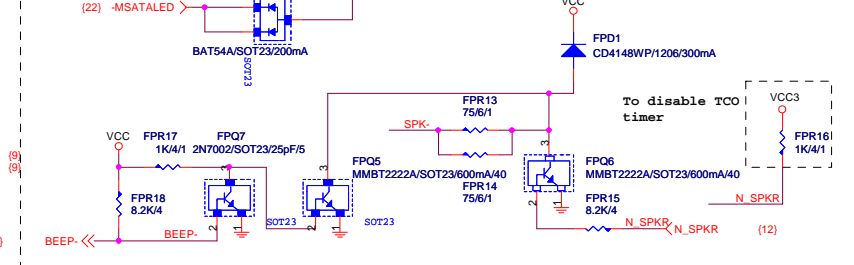
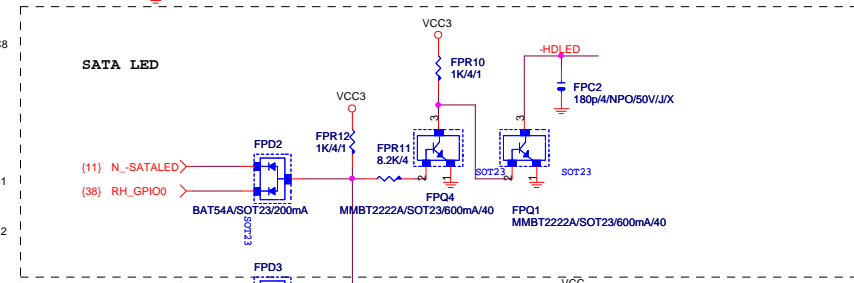
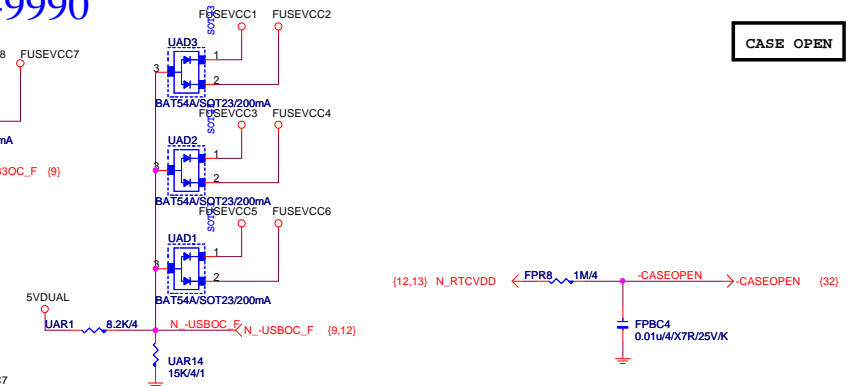
(39) RESET >>

(12,35) N_SYS_RST << FPR5 100u/4/1

INTEL FRONT PANEL



Close to connector

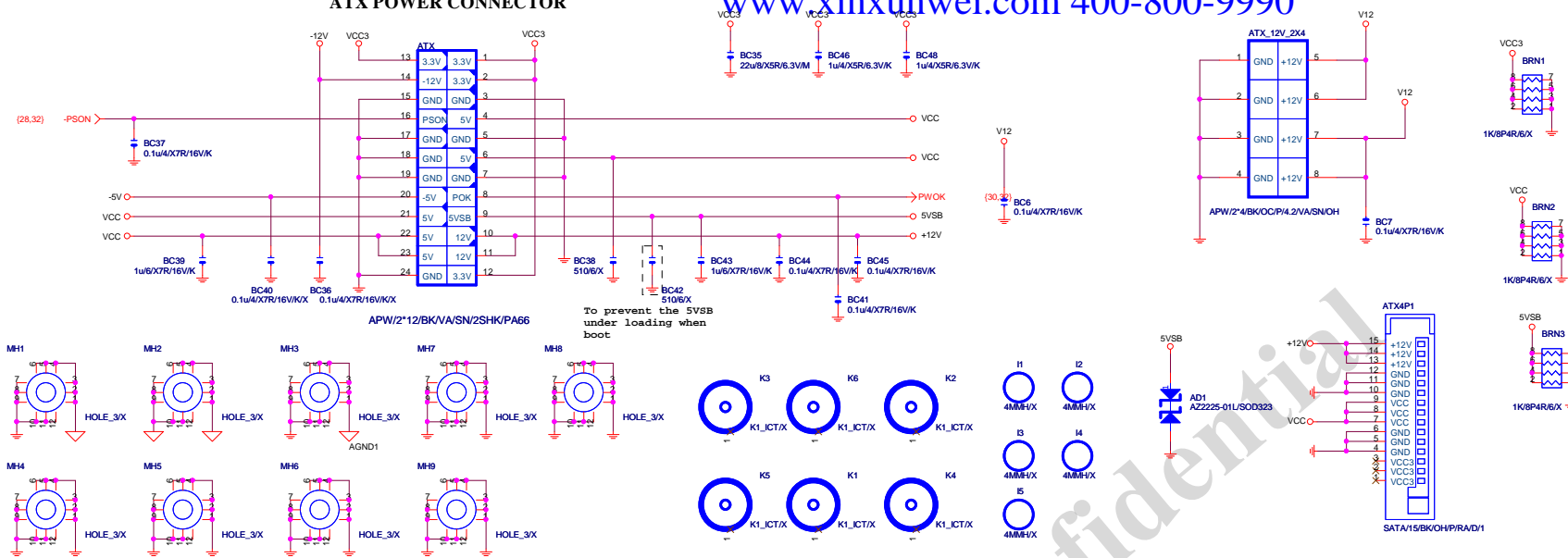


Gigabyte Technology

Title			FF.P_USB,BZ
Size	Document Number	GA-Z77X-UD3H	
Custom		Rev 1.03	
Date:	Wednesday, March 21, 2012	Sheet	34 of 41

ATX POWER CONNECTOR

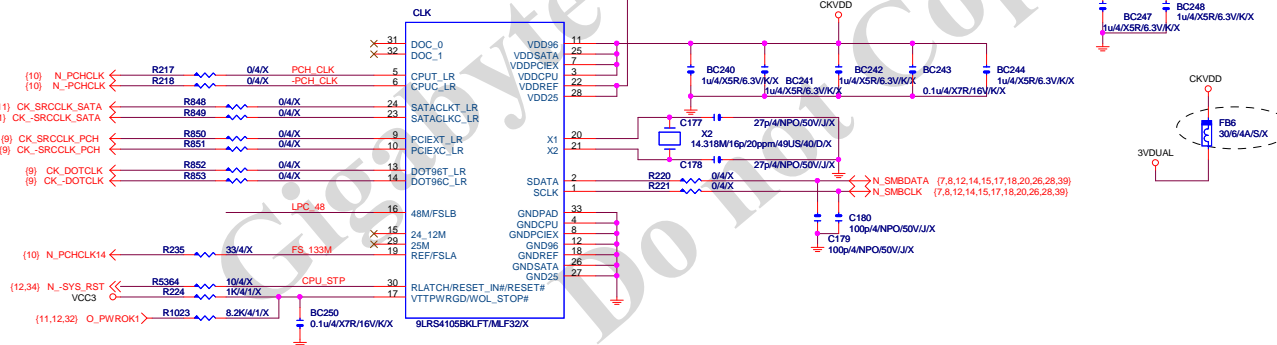
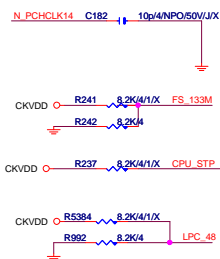
www.xinxunwei.com 400-800-9990



CLK GEN CK505

CPU Frequency Selection

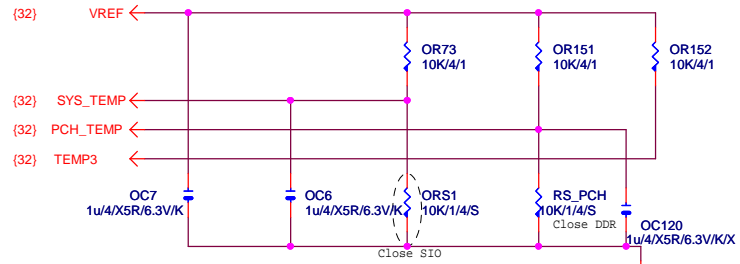
FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



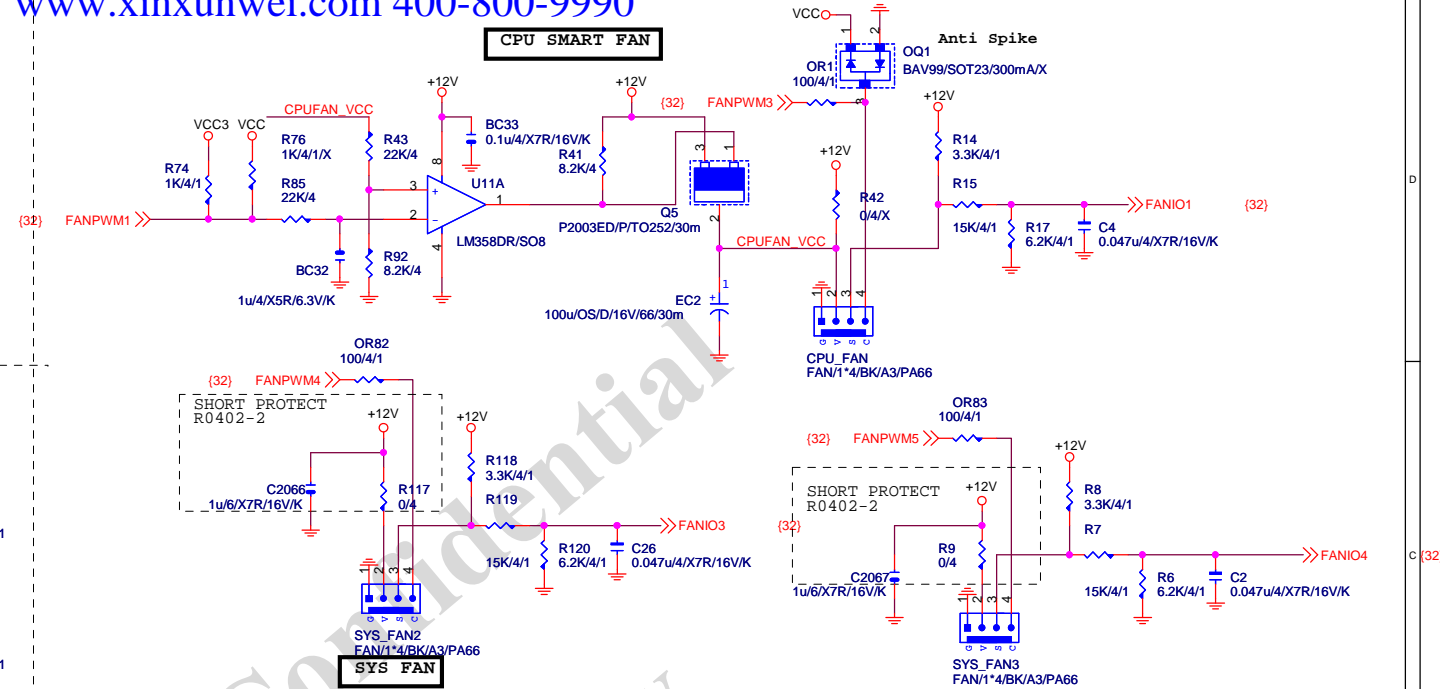
Gigabyte Technology

Title			Rev
ATX POWER CONNECTOR			1.03
Size	Document Number	GA-Z77X-UD3H	
Custom			
Date:	Wednesday, March 21, 2012	Sheet	35 of 41

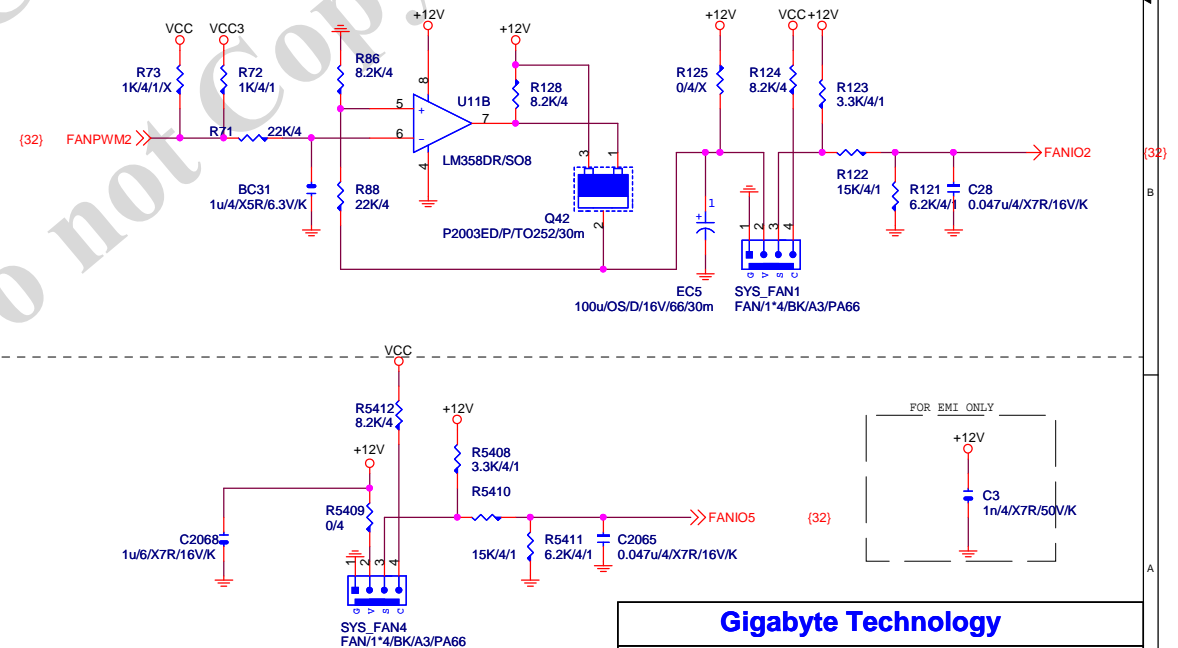
TEMP H/W MONITOR



CPU SMART FAN



Linear SYS_FAN



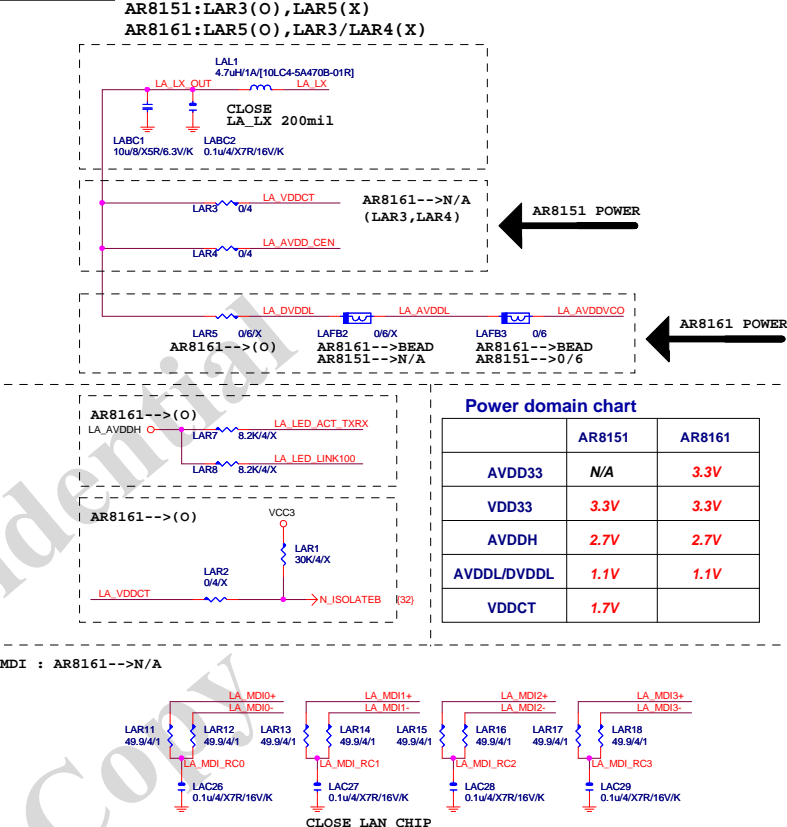
Gigabyte Technology

Title		
HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev
Custom	GA-Z77X-UD3H	1.03
Date:	Wednesday, March 21, 2012	Sheet 36 of 41

The division voltage of VIN2 & VIN3 must be around 2.9V

LAN POWER-NEW

LAN POWER-NEW



AR8151: LAR3(O), LAR5(X)
AR8161: LAR5(O), LAR3/LAR4(X)

LA L1
4.7uH/1A/10LC4-5A470B-01R

LA LX OUT

LA LX

CLOSE
LA_LX 200mil

LABC1
10u8/XSR/6.3VK

LABC2
0.1u4/X7R/16VK

LAR3 0/4

LA VDDCT

AR8161-->N/A
(LAR3, LAR4)

LA VDDCEN

LAR4 0/4

LA DVDDL

LAR5 0/6/X

AR8161-->(O)

LAFB2 0/6/X

AR8161-->BEAD
AR8151-->N/A

LAFB3 0/6

AR8161-->BEAD
AR8151-->0/6

LA DVDDL

LA VDDDL

LA VDDVCO

AR8161-->(O)

LA VDDH

LA LED ACT TXRX

LAR7 8.2K/4/X

LA LED LINK100

LAR8 8.2K/4/X

AR8161-->(O)

VOC3

LAR1 30K/4/X

LA VDDCT

LAR2 0/4/X

N_ISOLATEB [32]

Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A

LA MDIO+
LA MDIO-

LAR11 49.9/4/1

LAR12 49.9/4/1

LAR13 49.9/4/1

LA MDI_RC0

LAC26 0.1u4/X7R/16VK

LA MDI+
LA MDI-

LAR14 49.9/4/1

LAR15 49.9/4/1

LA MDI_RC1

LAC27 0.1u4/X7R/16VK

LA MDI2+
LA MDI2-

LAR16 49.9/4/1

LAR17 49.9/4/1

LA MDI_RC2

LAC28 0.1u4/X7R/16VK

LA MDI3+
LA MDI3-

LAR18 49.9/4/1

LA MDI_RC3

LAC29 0.1u4/X7R/16VK

CLOSE LAN CHIP

AR8151: LAR3(O), LAR5(X)
AR8161: LAR5(O), LAR3/LAR4(X)

LA L1
4.7uH/1A/10LC4-5A470B-01R

LA LX OUT

LA LX

CLOSE
LA_LX 200mil

LABC1
10u8/XSR/6.3VK

LABC2
0.1u4/X7R/16VK

LAR3 0/4

LA VDDCT

AR8161-->N/A
(LAR3, LAR4)

LA VDDCEN

LAR4 0/4

AR8151 POWER

LA DVDDL

LAR5 0/6/X

AR8161-->(O)

LAFB2 0/6/X

AR8161-->BEAD
AR8151-->N/A

LAFB3 0/6

AR8161-->BEAD
AR8151-->0/6

LA DVDDL

LA VDDVCO

AR8161 POWER

AR8161-->(O)

LA VDDH

LAR7 8.2K/4/X

LA LED ACT_TXRX

LAR8 8.2K/4/X

LA LED_LINK100

AR8161-->(O)

VOC3

LAR1 30K/4/X

N_ISOLATEB [32]

LA VDDCT

LAR2 0/4/X

Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A

LA MDIO+
LA MDIO-

LAR11 49.9/4/1

LAR12 49.9/4/1

LAR13 49.9/4/1

LA MDI_RC0

LAC26 0.1u4/X7R/16VK

LA MDI+
LA MDI-

LAR14 49.9/4/1

LAR15 49.9/4/1

LA MDI_RC1

LAC27 0.1u4/X7R/16VK

LA MDI2+
LA MDI2-

LAR16 49.9/4/1

LAR17 49.9/4/1

LA MDI_RC2

LAC28 0.1u4/X7R/16VK

LA MDI3+
LA MDI3-

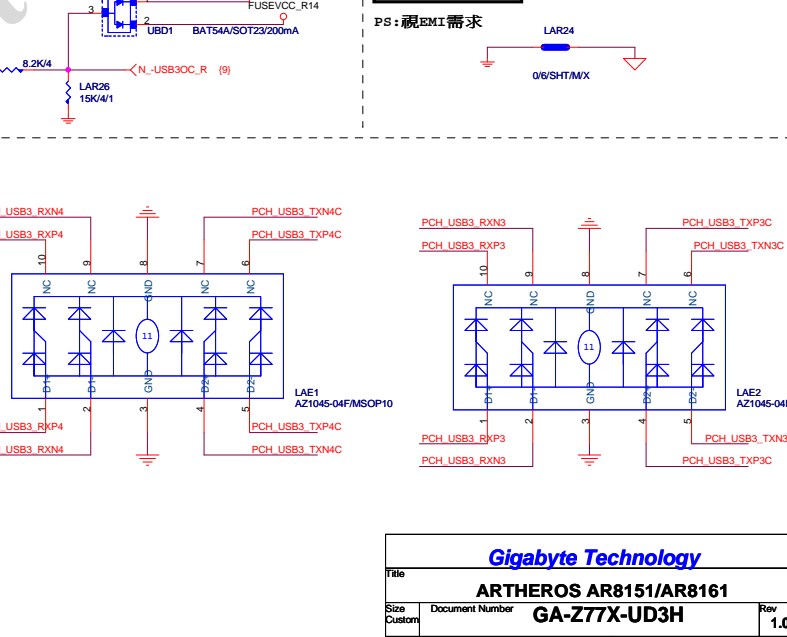
LAR18 49.9/4/1

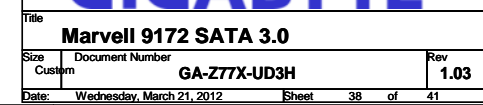
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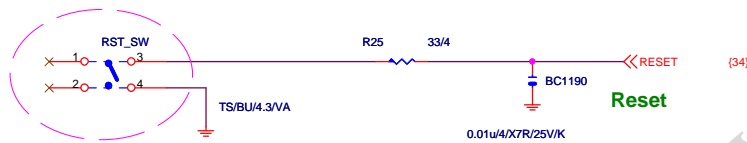
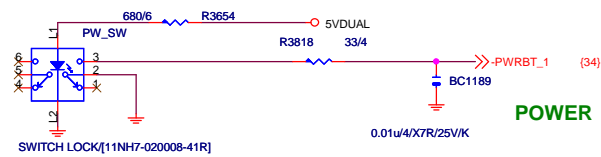
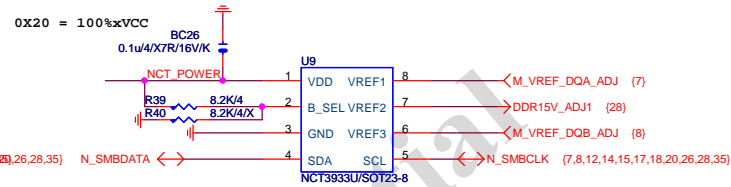
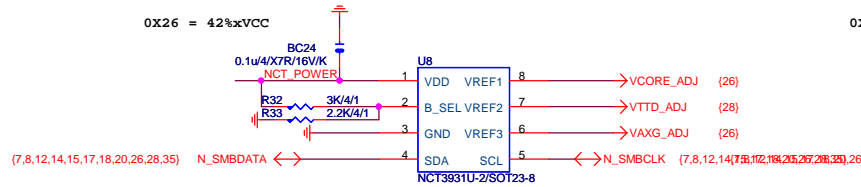
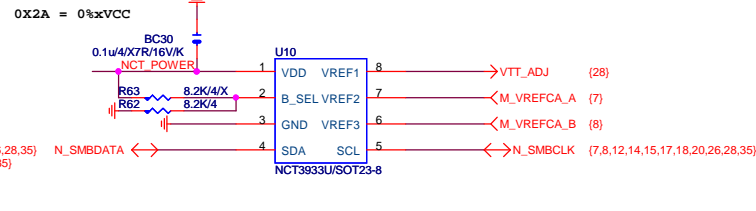
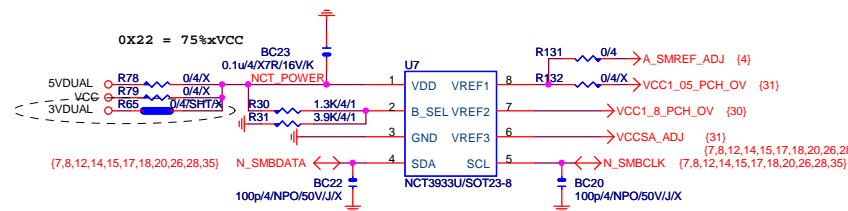
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CLOSE LAN CHIP

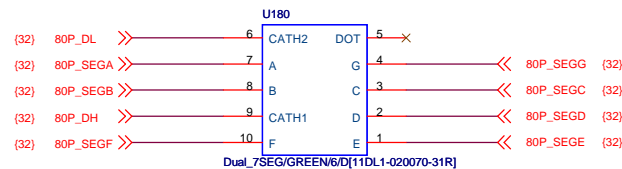
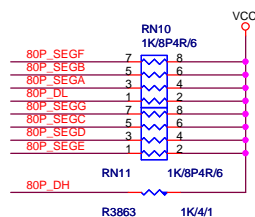
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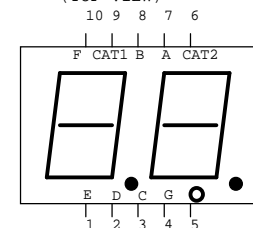


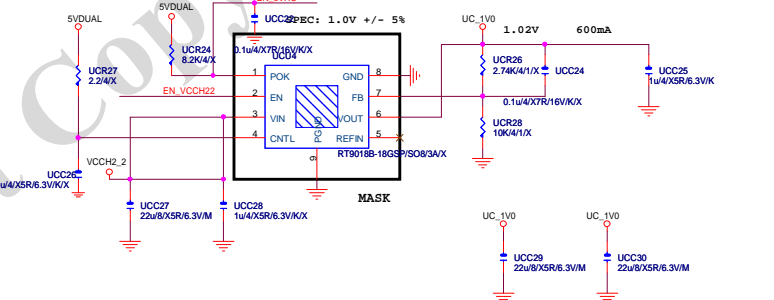
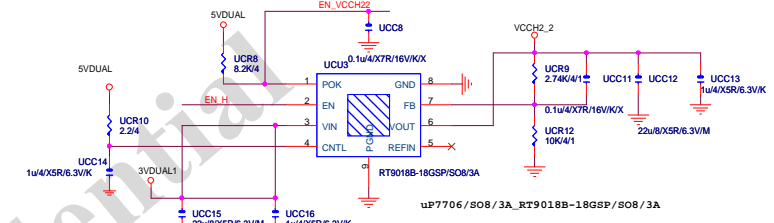
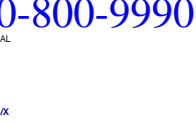
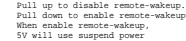


80 PORT



COMMON CATHODE

Physical Package
(TOP VIEW)

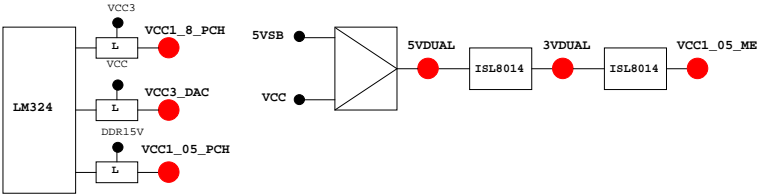


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

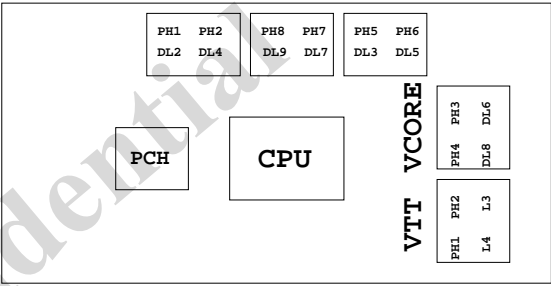
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CsisBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDVA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VIDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT15/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_AVREF_CA_B	DRAM Address Ref
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
TABLE LIST			
Size C	Document Number	Rev	
	GA-Z77X-UD3H	1.03	
Date:	Wednesday, March 21, 2012	Sheet	41 of 41